# Contents

## 1
### Introducing Constraint Manager
- The Constraint Manager Information Set .................................................. 7
- What is Constraint Manager? ........................................................................... 8
- A Quick Look at Constraint Manager Controls .................................................. 11
  - The Worksheet Selector ................................................................................ 11
  - Constraint Manager's User Interface Controls ................................................ 13
- Accessing Constraint Manager ........................................................................ 16
  - Constraint Manager launched from Allegro Designer .................................... 17

## 2
### Working with Objects
- Object Hierarchy ............................................................................................... 19
- Learning About Constraint Manager Objects ................................................... 20
  - Pin-Pair ........................................................................................................... 20
  - Net and Xnet .................................................................................................. 21
  - Bus .................................................................................................................. 22
  - Diff Pair ......................................................................................................... 23
  - Relative/Matched Group ............................................................................... 24
  - Design and System ....................................................................................... 25
- Working with Constraint Manager Objects ....................................................... 26
  - Working with Pin-Pairs .................................................................................. 26
    - Pin-Pair Rules ............................................................................................. 27
    - Operations on a Pin-Pair ............................................................................. 28
    - Examples of Pin-Pairs ............................................................................... 29
  - Working with Nets ........................................................................................... 29
    - Operations on a Net .................................................................................... 30
    - Total Etch Length ....................................................................................... 31
  - Working with Buses ......................................................................................... 32
    - Bus Rules .................................................................................................... 33
    - Operations on a Bus .................................................................................... 34
<table>
<thead>
<tr>
<th>Section</th>
<th>Title</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>Working With Constraints</td>
<td>41</td>
</tr>
<tr>
<td></td>
<td>Electrical Constraint Sets</td>
<td>42</td>
</tr>
<tr>
<td></td>
<td>Referencing ECSets</td>
<td>43</td>
</tr>
<tr>
<td></td>
<td>ECSet Rules</td>
<td>44</td>
</tr>
<tr>
<td></td>
<td>Working with ECSets</td>
<td>45</td>
</tr>
<tr>
<td></td>
<td>Operations on ECSets</td>
<td>47</td>
</tr>
<tr>
<td>4</td>
<td>ECSets and Topology Templates</td>
<td>51</td>
</tr>
<tr>
<td></td>
<td>What is a Topology Template?</td>
<td>52</td>
</tr>
<tr>
<td></td>
<td>Importing ECSets</td>
<td>54</td>
</tr>
<tr>
<td></td>
<td>Mapping Templates and ECSets to Net-related Objects</td>
<td>56</td>
</tr>
<tr>
<td></td>
<td>Auditing ECSets</td>
<td>59</td>
</tr>
<tr>
<td></td>
<td>Constraint Audit</td>
<td>59</td>
</tr>
<tr>
<td></td>
<td>Obsolete Objects Audit</td>
<td>60</td>
</tr>
<tr>
<td></td>
<td>Electrical CSets Audit</td>
<td>61</td>
</tr>
<tr>
<td></td>
<td>Topology Templates Audit</td>
<td>61</td>
</tr>
<tr>
<td></td>
<td>Exporting ECSets</td>
<td>64</td>
</tr>
<tr>
<td></td>
<td>Migrating Pre 14.0 Electrical Rule Sets</td>
<td>64</td>
</tr>
<tr>
<td>5</td>
<td>Constraint Analysis</td>
<td>65</td>
</tr>
<tr>
<td></td>
<td>How Constraint Manager Performs Analysis</td>
<td>66</td>
</tr>
<tr>
<td></td>
<td>Cell Colors used in Analysis</td>
<td>67</td>
</tr>
<tr>
<td></td>
<td>Viewing Worksheet Cells and Objects</td>
<td>69</td>
</tr>
<tr>
<td></td>
<td>Analyzing for Rule-based Constraints</td>
<td>72</td>
</tr>
<tr>
<td></td>
<td>Analyzing for Simulation-based Constraints</td>
<td>75</td>
</tr>
<tr>
<td></td>
<td>Custom Measurements and Custom Stimulus</td>
<td>76</td>
</tr>
</tbody>
</table>
The Analysis Process ............................................................................. 81
Analysis Results .................................................................................. 87
   Generated DRC Output ..................................................................... 87
   Waveforms ...................................................................................... 87
   Reports ............................................................................................. 88
   Worksheet cells ............................................................................... 88
Interpreting Analysis Results Returned to a Worksheet ......................... 89
Constraints Across the System ............................................................... 92

6
Using Constraint Manager in the High Speed Design Flow .................. 93
Phases in the Design Flow .................................................................... 94
Design Exploration Phase (with SigXplorer) .......................................... 95
   Pin Scheduling ............................................................................... 96
Design Capture Phase (with Concept HDL) ........................................... 97
   Using Constraint Manager with Concept HDL ............................... 98
   Front-to-Back Constraint Flow ..................................................... 103
   Back-to-Front Constraint Flow .................................................... 104
Design Floorplanning and Implementation Phases
   (with SPECCTRAQuest and Allegro) ............................................. 106
   Using SigXplorer in the capture, floorplanning and implementation phases .... 109

A
Migrating Pre 14.0 Electrical Constraints ............................................. 111
Overview ........................................................................................... 112
Managing Constraints in Release 13.6 ............................................... 112
   Electrical Rule Sets ....................................................................... 112
   Topology Templates ...................................................................... 113
   Net Properties .............................................................................. 113
Managing Constraints with Constraint Manager .................................. 114
   Electrical Rule Sets ....................................................................... 114
   The UPREVED_DEFAULT ECSets ............................................. 115
   Topology Templates ...................................................................... 115
B

Property Mapping ......................................................... 121

Overview ................................................................. 122

Workbooks under the ECSet folder .................................. 122
  Properties in the signal integrity workbook ...................... 122
  Properties in the Timing workbook ................................ 123
  Properties in the Routing workbook .............................. 124

Workbooks under the Net folder ..................................... 126
  Properties in the signal integrity workbook ...................... 126
  Properties in the timing workbook ................................ 127
  Properties in the routing workbook .............................. 129
1

Introducing Constraint Manager

Topics in this chapter include

- The Constraint Manager Information Set on page 8
- What is Constraint Manager? on page 8
- A Quick Look at Constraint Manager Controls on page 11
The Constraint Manager Information Set

The Constraint Manager information set consists of online help (WinHelp) and online books (in both HTML and PDF formats). All documentation is accessible from Constraint Manager's help menu.

Refer to . . . for this level of information

Constraint Manager Design Guide (this book)

This book is for users who want to know how to use Constraint Manager in the high-speed design flow.

This book can be viewed online in Cadence’s Product Documentation system and it can be printed using Adobe Acrobat’s® portable document format.

SPECCTRAQuest Simulation and Analysis Reference

This book contains reference information about the analysis engine used by Constraint Manager.

Constraint Manager Online Help

Online help contains procedures and provides information on using dialog boxes.

Online help is displayed in WinHelp.

What is Constraint Manager?

Constraint Manager is a cross-platform, workbook- and worksheet-based application used to manage high-speed electrical constraints across all tools in the Cadence PCB design flow.

Constraint Manager lets you define, view, and validate constraints at each step in the design flow, from design capture (in Concept HDL) to floorplanning (in SPECCTRAQuest expert) to design realization (in Allegro Expert, Allegro Designer, or Advanced Package Designer expert). You can also use Constraint Manager with SigXplorer Expert to explore circuit topologies and derive electrical constraint sets which can include custom measurements and custom stimulus.
Constraint Manager uses familiar user interface controls. See Table 1-2 on page 13 for more information.

Figure 1-1  The Constraint Manager User Interface

In Constraint Manager, you work with objects and electrical constraint sets (ECSets). You define one or more ECSets to capture your design requirements in the form of electrical constraints. You then assign the appropriate ECSR to objects in your design, swapping ECSR assignments (or re-defining the currently assigned ECSR) as your design requirements change. An ECSR can be referenced by any number of objects in your design. Objects and ECSR can be generic to the entire design or they can reference a specified net in the design.

For more information on design objects and the object hierarchy, see Chapter 2, “Working with Objects.”

For more information on how to define ECSR and how to assign them to objects in your design, see Chapter 3, “Working With Constraints.”

Constraint Manager affords you the following features and benefits:
Table 1-1 Constraint Manager Features

<table>
<thead>
<tr>
<th>Feature</th>
<th>Benefit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Object Grouping</td>
<td>You can organize objects into easily-managed units, such as a bus or a match set, to make it easier to apply constraints to member objects.</td>
</tr>
<tr>
<td>Conceptual Definition</td>
<td>You can define constraints conceptually and later apply those constraints to physical, net-related objects.</td>
</tr>
<tr>
<td>Redefinable Constraints</td>
<td>Rather than changing individual net-related constraints one-by-one, you can redefine an ECSet and all objects that reference that ECSet get updated all at once.</td>
</tr>
<tr>
<td>Cross-Probing</td>
<td>■ You can run Constraint Manager with companion tools such as Concept HDL, SPECCTRAQuest, or Allegro/APD and select a net in Constraint Manager and see the associated object update dynamically in the schematic, floorplanner, or layout, respectively.</td>
</tr>
<tr>
<td></td>
<td>■ Conversely, Constraint Manager updates its values when they are modified in a companion tool.</td>
</tr>
<tr>
<td>Topology Exploration</td>
<td>■ When you cross-probe cells that contain constraint violations, the respective DRC marker (bowtie) becomes highlighted in SPECCTRAQuest, Allegro, or APD.</td>
</tr>
<tr>
<td></td>
<td>You can access SigXplorer from Constraint Manager to schedule pins and derive generic or net-specific constraints, which may include custom measurements and custom stimulus. The resulting topology template data can be imported into Constraint Manager as an ECset.</td>
</tr>
<tr>
<td>Design Reuse</td>
<td>You group constraints that satisfy a specific design requirement into an ECSet which can be referenced within the active design or exported for reuse in a subsequent design.</td>
</tr>
<tr>
<td>Cloning Constraints</td>
<td>In addition to importing ECSets or creating ECSets from scratch, you can copy an ECSet, modify its parameters, and save it under a new name.</td>
</tr>
<tr>
<td>Analysis</td>
<td>Constraint Manager performs design rule checks, and simulations as necessary, to analyze the design. Analysis results are communicated by DRC markers, results populated in worksheet cells, simulation waveforms, and reports.</td>
</tr>
<tr>
<td></td>
<td>Analysis results (actuals) can be compared to defined constraints to derive margins.</td>
</tr>
<tr>
<td>System-level Constraints</td>
<td>Constraint Manager can capture board-to-board interconnect constraints.</td>
</tr>
</tbody>
</table>
A Quick Look at Constraint Manager Controls

The Constraint Manager workspace (Figure 1-1 on page 9) contains the following components:

- Command access through menu and icon selection
- The worksheet selector for selecting the appropriate worksheet
- The worksheets for capturing, editing, and validating constraints
- The status bar for feedback on object selection and constraint processing

**Note:** When you select an object in Constraint Manager and click-right, you can also access commands from the context-menu.

The Worksheet Selector

You use the worksheet selector to access the appropriate worksheet that you want to work in.

Object Type Folders

In Constraint Manager, the worksheet selector organizes constraints and properties by object type. Object types are represented by the top-most (parent-level) folders Electrical Constraint Set and Net.
Figure 1-2  Object Types and Workbooks

In the Electrical Constraint Set folder, you define generic rules and you create generic object groupings (relative or match group, and pin-pair). You can later assign these rules—an ECSet—to the appropriate net-related objects in your design.

In the Net folder, you create net-specific object groupings (system, design, bus, diff-pair, Xnet, net, relative or match group, and pin-pair). You can also create an ECSet based on the characteristics of a net-related object. This ECSet will then reside in the Electrical Constraint Set folder.

Workbooks

Once you expand an Electrical Constraint Set or Net object folder, workbooks organize objects by design discipline: Signal Integrity, Timing, Routing, and Custom Measurements. Additionally, there is an All Constraints workbook which consolidates constraints from all worksheets to give you a global view.

Important

Typically, you define an ECSet when you are working in a specific worksheet. Therefore, this ECSet is relevant only to the active worksheet and not other worksheets. You can define an ECSet in the All Constraints workbook which, by definition, spans all worksheets in all workbooks. In this way, you can make sweeping, design-level constraint definitions at once, rather than one definition after another. The All Constraints worksheet is also useful for comparing (or editing) constraints from different worksheets.

Net-related worksheets also contain cells for Actual and Margin calculations.

When you select a workbook, all worksheets that belong to that workbook appear in a shared worksheet window. You can use the worksheet selector to select a worksheet or you can select a worksheet by clicking on the appropriate tab in the shared workbook window. You may have to scroll horizontally to locate the desired worksheet tab.

Note: When you launch Constraint Manager from a layout tool, the cells that are in view are populated first. As you scroll other cells into view, the layout tool updates hidden cells as they become visible in Constraint Manager.
In Figure 1-3, notice how the Net object folder is expanded to show Timing as the active workbook. The Timing workbook contains the Switch/Settle Delays and Setup/Hold worksheets. Notice how the worksheets in the worksheet selector correspond to the worksheet tabs in the active workbook. Also notice that the active workbook and the active worksheet within the active workbook are emphasized with color in the workbook selector.

For information on objects and the object hierarchy, see Chapter 2, “Working with Objects.” For information on how to define ECsets and how to assign them to objects in your design, see Chapter 3, “Working With Constraints.”

**Constraint Manager’s User Interface Controls**

Constraint Manager employs the same conventional window and worksheet controls that are used in Microsoft Windows 2000 Explorer® and Microsoft Excel®.

### Table 1-2 User Interface Controls

<table>
<thead>
<tr>
<th>Task</th>
<th>Feature</th>
<th>Usage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Command Access</td>
<td>Pull-down Menus</td>
<td>Click the pull-down menu at the top of Constraint Manager to access commands.</td>
</tr>
<tr>
<td></td>
<td>Icons</td>
<td>Click an icon to execute a command.</td>
</tr>
</tbody>
</table>

If you briefly hover the cursor above an icon, a tool tip displays in the status bar (located at the lower-left corner of Constraint Manager) describing the icon’s function.
## Task

### Feature

<table>
<thead>
<tr>
<th>Task</th>
<th>Feature</th>
<th>Usage</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Keyboard Shortcuts</td>
<td>Press <strong>Control</strong> and press:</td>
</tr>
<tr>
<td></td>
<td>p (to print)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>z (to undo)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>c (to cut)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>v (to paste)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>f (to find)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>d (to delete)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Also, you can access many commands by pressing <strong>Alt</strong> along with the underlined character.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Click-Right (context sensitive)</td>
<td>Depending on the object selected, you can click-right to quickly access a command to act on that object.</td>
</tr>
<tr>
<td>Window and Worksheet Sizing and Placement</td>
<td>Drag and Drop</td>
<td>You can drag to reposition the Constraint Manager window, and individual worksheets, on your desktop.</td>
</tr>
<tr>
<td></td>
<td>Sizing Borders</td>
<td>You can resize the Constraint Manager window or an individual worksheet open within Constraint Manager by dragging the border.</td>
</tr>
<tr>
<td></td>
<td>Maximize/Minimize</td>
<td>You can minimize an open worksheet to an icon or you can maximize it to focus only on that worksheet.</td>
</tr>
<tr>
<td></td>
<td>Dismiss</td>
<td>You can click the dismiss [X] button (located at the top right-corner of the worksheet) to close a worksheet. Constraint data is not lost when you dismiss a worksheet.</td>
</tr>
<tr>
<td>Worksheet Viewing</td>
<td>Window Select</td>
<td>You can click and drag on an open worksheet to reposition it.</td>
</tr>
</tbody>
</table>
## Task Feature Usage

<table>
<thead>
<tr>
<th>Task</th>
<th>Feature</th>
<th>Usage</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Object Expand/Collapse</td>
<td>You can use the worksheet selector to work at any object level in the hierarchy (from the system level to the pin-pair level) by expanding [+] and collapsing [-] the object tree-structure. You can also choose <em>Objects – Expand</em> and <em>Objects – Collapse</em> from the pull-down menus to achieve the same effect.</td>
</tr>
<tr>
<td></td>
<td>Cascade</td>
<td>You can view all open worksheets arranged one-behind-the-other by cascading (<em>Window – Cascade</em>). Constraint Manager orders Worksheets so that each is selectable with a click of the mouse. The active window is placed in the foreground and is identifiable by an active (selected) border.</td>
</tr>
<tr>
<td></td>
<td>Tile</td>
<td>You can view all open worksheets simultaneously by tiling (<em>Window – Tile</em>). Each open worksheet is automatically sized to accommodate the size of the Constraint Manager window.</td>
</tr>
<tr>
<td></td>
<td>New Window</td>
<td>You can duplicate the content of the active worksheet in a new window. This lets you to focus your view on different objects in the same worksheet.</td>
</tr>
<tr>
<td></td>
<td>Worksheet Tab Select</td>
<td>When you expand a constraint discipline (signal integrity, timing, routing) from the worksheet selector, all objects within that discipline appear in a worksheet window. You then click a related tab to activate the desired worksheet. You may have to scroll horizontally until the desired worksheet tab is visible.</td>
</tr>
</tbody>
</table>
Accessing Constraint Manager

You access Constraint Manager in stand-alone mode through the Windows Start menu or by entering `consmgr` in a Unix shell.

Constraint Manager can also be invoked from a host tool as follows:

<table>
<thead>
<tr>
<th>From this tool</th>
<th>Choose this menu command</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECCTRAQuest, Allegro, or APD</td>
<td>Setup – Electrical Constraint Spreadsheet</td>
</tr>
<tr>
<td>Concept HDL</td>
<td>Tools – Constraints – Edit</td>
</tr>
<tr>
<td></td>
<td>-or-</td>
</tr>
<tr>
<td></td>
<td>Tools – Constraints – Update Schematic</td>
</tr>
</tbody>
</table>

You can also click the Constraint Manager icon in the host tool’s toolbar.

When Constraint Manager is called from Allegro Expert, Allegro Designer, Advanced Package Designer Expert, SPECCTRAQuest SI Expert, or Concept HDL, the constraint information is saved with the board database or a constraints view.

The name of the tool from which you launch Constraint Manager appears in the banner atop the Constraint Manager user interface. For example:

Constraint Manager (Connected to Concept HDL)

See Chapter 6, “Using Constraint Manager in the High Speed Design Flow” for using Constraint Manager with other Cadence tools.
Constraint Manager Design Guide
Introducing Constraint Manager

Constraint Manager launched from Allegro Designer

Constraint Manager affords Allegro Designer users with a convenient method of defining diff pairs. When invoked from Allegro Designer, Constraint Manager launches with a limited functionality set. This design guide is written with the Allegro Expert user in mind; all functionality in Constraint Manager is covered. As such, if you invoke Constraint Manager from Allegro Designer, you should be aware of the following limitations:

- **Scripting**
  Scripting is limited to the commands and constraints that are supported in Allegro Designer.

- **Match Groups**
  Match Groups can be defined only in worksheets in the Nets folder; you cannot define match groups in workbooks at the ECSet-level.

- **Pin-pairs**
  Pin-pairs can be defined only in worksheets in the Nets folder; you cannot define pin-pairs in workbooks at the ECSet-level.

- **Signal Integrity**
  Signal integrity analysis is not supported. The Signal Integrity workbook has been removed.

- **Timing**
  Timing analysis is not supported. The Timing workbook has been removed.

- **Custom measurements and custom stimulus**
  Custom measurements and custom stimulus are not supported. The custom measurements tab (Analyze – Analysis Modes) has been removed; only the DRC Modes tab remains. The custom measurements workbook is also hidden.

- **Crosstalk DRC**
  Crosstalk analysis is not supported. The \text{max xtalk} and \text{max peak xtalk} design rule checks have been removed from the Analysis Modes dialog box.

- **Topology Templates**
  Topology (ECSet) import and export are not supported. As such, the Tools menu has also been removed prohibiting access to topology exploration tools including SigXplorer, SigWave, and EMwave.

- **Analysis**
  Simulation-based analysis is not supported. Only design rule checks can be performed.

When you select an object in Constraint Manager and click-right, a context pop-up menu appears. Keep in mind that this guide depicts all available options. If you launched Constraint Manager from Allegro Designer, some options will be removed or dimmed to inhibit functionality.
Working with Objects

Topics in this chapter include

- Object Hierarchy on page 20
- Learning About Constraint Manager Objects on page 22
- Working with Constraint Manager Objects on page 26
- Refer to Constraint Manager online help for step-by-step procedures, on page 26
- Working with Buses on page 34
- Working with Match Groups on page 37
Object Hierarchy

Constraint Manager enforces a precedence on objects in your design; the top-most object is the System, the bottom-most object is the pin-pair. For descriptions of allowable objects and object groupings in Constraint Manager, see “Learning About Constraint Manager Objects” on page 22.

Constraints that you specify at the top of the object hierarchy become inherited by the next lower-level object in the hierarchy.

Constraints that you define at the lower-levels of the object hierarchy take precedence over (override) the same constraints defined at the next higher-level in the object hierarchy.

Note: The object hierarchy graphic depicts net-related object types. Electrical Constraint Set object types do not include net related information (Xnet and Net) but follow the same precedence as Net object types.

This ordering of objects lets you define constraints at highest level possible only setting overrides on lower-level objects where necessary.

Note: In certain worksheets, the children of an object reflect the results of an analysis and are not used for the constraint precedence hierarchy. These result-objects are not differentiated from the normal constraint hierarchy but will be maintained for reading. You cannot edit these constraints.

Figure 2-1 depicts a multi-board system configuration consisting of a motherboard, A_TO_B, and two daughter board designs, A and B. Also included are net, Xnet, diff-pair, pin-pair, and bus object groupings.
Figure 2-1 A Sample Multi-board Object Hierarchy

[-] A_TO_B  (System)
  [-] A:RAS0  (Xnet)
  A.U1.1:B.U33.2  (Pin Pair)
  [+ ] A:CAS0  (Xnet)

[-] A  (Design)
  [-] AddressBus  (Bus)
    [-] DP1  (Diff Pair)
      [-] Addr0-  (Xnet)
        U2.1:U4.1  (Pin Pair)
      [+ ] Addr0+  (Xnet)
    [+ ] DP2  (Diff Pair)
    [+ ] DP3  (Diff Pair)

...  

[-] DataBus  (Bus)
  [+ ] Data0  (Xnet)
  [+ ] Data1  (Xnet)
  [+ ] Data2  (Xnet)

...  

[+ ] DP35  (Diff Pair which is not part of a bus)

[+ ] control1  (Xnet which is not part of a bus of Diff Pair)
U33.1:U34.2  (Pin Pair)
U33.1:U35.2  (Pin Pair)
U33.1:U36.2) (Pin Pair)
[+ ] AA1  (Net which is not part of an Xnet)

[+ ] B  (Design)
Learning About Constraint Manager Objects

This section describes objects and object groupings that can exist in Constraint Manager.

**Pin-Pair**

A *pin-pair* represents a pair of logically connected pins, often a driver-receiver connection. Pin-pairs may not be directly connected but they must exist on the same net or Xnet.

**Note:** The Concept HDL database does not support pin-pair objects.

You may specify pin-pairs explicitly (for example, **U1.8 U3.8**), or they can be derived based on the following criteria:

- longest pin-pair
- longest driver-receiver pair
- all driver-receiver pairs

Longest driver/receiver: **U1.8 - U3.8**

**Net and Xnet**

A *net* represents an electrical connection from one pin to another pin (or pins) on the same device or on a different device.
Note: The Concept HDL database does not support Xnet objects.

If the path of a net traverses a passive, discrete device (resistor, inductor or capacitor), then each net segment is represented by an individual net entity in the board database. Constraint Manager, however, interprets these net segments as a contiguous extended net, or an Xnet. An Xnet can also traverse connectors and cables in a multi-board configuration.

Bus

A bus represents a named collection of diff-pairs, Xnets, or Nets. Grouping objects, such as with creating a bus, makes it easier to apply and manage constraints on similar nets.

Diff Pair

A diff-pair (electrical differential pair) represents a pair of Xnets or nets which will be routed differentially. The opposite signals of the pair, which share the same reference, cancel out any electromagnetic noise in the circuit.

Diff-pairs are created automatically based upon signal model assignments. The signal model defines the appropriate pin characteristics. You assign signal models to devices using Allegro, SPECCTRAQuest, or SigXplorer.
Relative/Matched Group

A Relative/Matched (propagation) group represents a user-specified collection of pin-pairs constrained by a relative or match delay or length.

In this illustration two of the three nets belong to a relative group—M1. To maintain a match propagation delay, the middle net is extended to match the length of the bottom net.

The following attributes are used to characterize the requirements for a Relative/Match group:

- **Target**: The pin-pair that is referenced by all pin-pairs in the group. A pin-pair can be explicitly defined as the target in which case all other pin-pairs will then be compared to this target.
- **Delta**: The difference between each pin-pair member and the target pin-pair. If the delta is zero, all members need to match.
- **Tolerance**: The skew allowed when matching members in the group.

Determining the target pin-pair

One of the pin-pairs is selected as the target and all of the other pin-pairs will be matched against this target within the given delta and tolerance.

Constraint Manager determines the target pin-pair as follows:

1. The pin-pair that you explicitly set (using the right mouse button).
2. If all pin-pairs have a delta value, the pin-pair with the smallest delta value is selected as the target. If more than one pin-pair has the same (smallest) delta value, the pin-pair with the longest length is selected as the target.
3. If none of the pin-pairs has a delta value, then there is no target selected. All pin-pairs are compared to each other (pre-14.0 match delay check).
Relative/Matched Delay Scenarios

The following table illustrates how Constraint Manager processes relative/match delay groups. Assume a match group with the following pin-pairs:

<table>
<thead>
<tr>
<th>pin 1</th>
<th>pin2</th>
<th>delta</th>
<th>tolerance</th>
</tr>
</thead>
<tbody>
<tr>
<td>U1.1</td>
<td>U2.2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>U3.3</td>
<td>U4.4</td>
<td>300 mils</td>
<td>10%</td>
</tr>
<tr>
<td>U5.5</td>
<td>U6.6</td>
<td>-0.5 ns</td>
<td></td>
</tr>
<tr>
<td>U7.7</td>
<td>U8.8</td>
<td>0.3 ns</td>
<td>0.1 ns</td>
</tr>
<tr>
<td>U9.9</td>
<td>U10.10</td>
<td>0 mils</td>
<td>5%</td>
</tr>
</tbody>
</table>

Pin-pair U1.1-U2.2 will be selected as the target because there is not a delta value specified. All other pin-pairs will be compared against this target.

The U3.3-U4.4 pin-pair has a delta of 300 mils and a tolerance of 10%. This indicates that the connection between this pin-pair must be 300 mils longer than the connection between the target pin-pair within a tolerance of +/- 10% (30 mils). In other words, the U3.3-U4.4 connection must be 270 mils to 330 mils longer than the U1.1-U2.2 connection.

The U5.5-U6.6 pin-pair has a -0.5 ns delta. Because it does not have an explicit tolerance value, a tolerance of 5% is assumed. This pin-pair is specified to be 0.5 ns shorter than the U1.1-U2.2 connection within a tolerance of +/- 0.025 ns. The U7.7-U8.8 pin-pair is specified to be 0.2 ns longer than the U1.1-U2.2 connection within a +/- 0.1 ns tolerance.

The U9.9-U10.10 pin-pair has a zero mils delta value with a 5% tolerance. This indicates that this pin-pair is specified to be the same length as the U1.1-U2.2 pin-pair. In this case the tolerance of the match is +/- 5% of the total length of U1.1-U2.2. If the delta value had been 0 ns, then the match would have been +/- 5% of the total delay of U1.1-U2.2.
Design and System

A design represents a stand-alone board or a board in a system. In a multi-board configuration, each board becomes a separate design in the system.

A system represents a configuration of designs (boards) including Xnets that traverse these designs and their interconnecting cables and connectors.

Working with Constraint Manager Objects

The next sections describe the operations that you can perform on the following objects:

- pin-pair
- net
- bus
- match group

Refer to Constraint Manager online help for step-by-step procedures.
Working with Pin-Pairs

You use pin-pairs to capture specific pin-to-pin constraints for a net or an Xnet. You can also use pin-pairs to capture generic pin-to-pin constraints for ECSets. Generic pin-pairs are used to automatically define net- or Xnet-specific pin-pairs when the ECSet is referenced.

Once established, a pin-pair is associated with an ECSet. See Chapter 3, “Working With Constraints” for information about creating ECSets and associating them with objects.

Pin-Pair Rules

The following rules apply to creating pin-pairs:

- Pin-pairs can only be defined in the following worksheets:

<table>
<thead>
<tr>
<th>Workbook</th>
<th>Worksheet</th>
</tr>
</thead>
<tbody>
<tr>
<td>All Constraints</td>
<td>Signal Integrity/Timing/Routing</td>
</tr>
<tr>
<td>Timing</td>
<td>Switch/Settle Delays</td>
</tr>
<tr>
<td></td>
<td>Setup/Hold</td>
</tr>
<tr>
<td>Routing</td>
<td>Impedance</td>
</tr>
<tr>
<td></td>
<td>Min/Max Propagation delay</td>
</tr>
<tr>
<td></td>
<td>Relative Propagation Delay</td>
</tr>
</tbody>
</table>

**Note:** Constraint Manager, when launched from Allegro Designer, does not support the Signal Integrity and Timing worksheets.

- Pins must exist in the object from which you create the pin-pair.
- Objects in the All Constraints and Timing worksheets must have a driver and a receiver as pin-pairs.
- Pin-pair length is the length of the etch path between the two pins, if the pins are routed. If not routed, the total manhattan distance of the ratsnest lines connecting the pins is used.
Constraint Manager determines longest/shortest pin-pair length based on drivers and receivers. If there are not any drivers or receivers, all pins in an Xnet are considered.

For a relative propagation delay constraint, only the longest pin-pair is determined.

User-defined pin-pairs are ignored.
## Operations on a Pin-Pair

This section summarizes pin-pair operations. Refer to the online help for detailed, step-by-step instructions.

### Table 2-1  Operations on Pin-Pairs

<table>
<thead>
<tr>
<th>Operation</th>
<th>Command</th>
</tr>
</thead>
<tbody>
<tr>
<td>Create a pin-pair</td>
<td>- Select a pair of nets or Xnets, then choose <em>Objects – Create – Pin Pair</em></td>
</tr>
<tr>
<td></td>
<td>- or –</td>
</tr>
<tr>
<td></td>
<td>- Select a pair of nets or Xnets, then click-right and choose <em>Create – Pin Pair</em> from the pop-up menu</td>
</tr>
<tr>
<td>Delete a pin-pair</td>
<td>- Select a pin-pair, then choose <em>Objects – Delete</em></td>
</tr>
<tr>
<td></td>
<td>- or –</td>
</tr>
<tr>
<td></td>
<td>- Select a pin-pair, then press <em>Delete</em></td>
</tr>
<tr>
<td>Create a Matched Group based on an existing pin-pair</td>
<td>- Select a pin-pair, then choose <em>Objects – Create – Matched Group</em></td>
</tr>
<tr>
<td></td>
<td>- or –</td>
</tr>
<tr>
<td></td>
<td>- Select a pin-pair, then click-right and choose <em>Create – Matched Group</em> from the pop-up menu</td>
</tr>
<tr>
<td>Select/Deselect a pin-pair in Allegro or SPECCTRAQuest</td>
<td>- Select a pin-pair, then choose <em>Objects – Select (or Deselect)</em></td>
</tr>
<tr>
<td></td>
<td>- or –</td>
</tr>
<tr>
<td></td>
<td>- Select a pin-pair, then click-right and choose <em>Select (or Deselect)</em> from the pop-up menu</td>
</tr>
<tr>
<td>Locate a pin-pair</td>
<td>- Choose <em>Edit – Find</em>, select pin-pair from the drop-down menu, then enter a pin-pair designation</td>
</tr>
<tr>
<td></td>
<td>- or –</td>
</tr>
<tr>
<td></td>
<td>- Choose <em>Objects – Filter</em>, then set the filter type to pin-pair. Next, enter a string to in which to search.</td>
</tr>
</tbody>
</table>
Examples of Pin-Pairs

Figure 2-2 shows two examples of creating pin-pairs. In the top example, a single, one-to-one pin map is specified on Net 5 (J1, Pin 1 to U2, Pin 3). In the bottom example, all permutations of pin mappings is realized. If all first pins and all second pins are selected, Constraint Manager maps all source pins to all target pins while excluding each pin combination that appears in both lists.

Figure 2-2  Example Pin-Pairs

Important
Use SHIFT-click to select a range of pins in the pin list or Control-click to selectively select pins.
Working with Nets

You use nets to capture constraints for electrical connections that exist on the same device (net) or between different devices (Xnet).

A net is associated with an ECSets. See Chapter 3, “Working With Constraints” for information about creating ECSets and associating them with objects.

Operations on a Net

This section summarizes net / Xnet operations. Refer to the online help for detailed, step-by-step instructions.

Table 2-2 Operations on Nets

<table>
<thead>
<tr>
<th>Operation</th>
<th>Command</th>
</tr>
</thead>
</table>
| Create an ECSets based on an existing net.    | - Select a net, then choose
|                                                |   Objects – Create – Electrical CSet
|                                                |   - or -
|                                                | - Select a net, then click-right and choose
|                                                |   Create – Electrical CSet from the pop-up menu |
| Select / Deselect a net or Xnet in Allegro or SPECCTRAQuest | - Select a net object in the worksheet, then choose
|                                                |   Objects – Select (or Deselect)
|                                                |   - or -
|                                                | - Select a net object in the worksheet, then click-
|                                                |   right and choose
|                                                |   Select (or Deselect) from the pop-up menu |
| Locate a net or Xnet                          | - Choose Edit – Find, select net from the drop-
|                                                |   down menu, then enter a net / Xnet designation
|                                                |   - or -
|                                                | - Choose Objects – Filter, then set the object types
to net or Xnet. Next, enter a string to search on.
Total Etch Length

You use the Total Etch Length worksheet to manage the minimum and maximum Total Etch Length constraints on each net / Xnet in the design. You can accomplish this with the design in either a routed or an unrouted state. See “Managing Total Etch Length Constraints”.

Managing Total Etch Length Constraints

Unrouted Designs

You can view and visually compare the unrouted manhattan length of Net(s) using the following procedure.

1. Right click in the header of the Unrouted Net Length column and choose the Analyze option to populate the fields with values.

2. Right click in the header of the Unrouted Net Length column and choose the Sort option to sort the length values.

The sorted column can now be used to view the longest Net(s) in the design. If a maximum Total Etch Length constraint is specified, the unrouted length can be used as a guideline for placement.
Routed Designs

After the design is routed, you can sort on the Margin column for either the Min or the Max constraint to find the worst offenders. Each maximum offender could be compared with its Routed/Unrouted Ratio to see if etch could be easily removed.

**Note:** A high ratio implies that extra etch was used to complete the route.

Alternatively, the 'Routed/Unrouted Ratio' column can be sorted to view the Nets which have high ratios. Nets with higher ratios could be scrutinized for poor routing (wandering) which could potentially inhibit 100% completion for the entire design.
Working with Buses

A bus is used to group functionally similar nets, Xnets, and diff pairs. Constraints captured on a bus will be inherited by all members of the bus.

Figure 2-4  Bus Inheritance

An ECSet can be created based on the characteristics of a bus. SigXplorer can then be used to define pin scheduling of bus members and to augment constraint information. When you associate the ECSet with a bus, all members (bits) of the bus inherit the constraints defined in the ECSet. In Figure 2-4, the VIDEO_DATA_CSET ECset is referenced to BUS (NETS 3, 4, 5). Each member of the bus inherits the properties defined in this ECSet.

See Chapter 3, “Working With Constraints” for information about creating ECSets and associating them with objects

See Chapter 6, “Using Constraint Manager in the High Speed Design Flow” for information on using SigXplorer.

Bus Rules

The following rules apply to creating a bus

- A bus can be created in all net-related worksheets
- When used in conjunction with Concept HDL, Constraint Manager cannot create a bus.
  A bus is only realized with the appropriate property in the schematic
- A bus must be at the design-level (not the system-level).
Operations on a Bus

This section summarizes bus operations. Refer to the online help for detailed instructions.

<table>
<thead>
<tr>
<th>Operation</th>
<th>Command</th>
</tr>
</thead>
</table>
| Create a bus | Select nets, Xnets, or diff pairs, then choose *Objects – Create – Bus*  
  - or -  
  Select a nets, Xnets, or diff pairs, then click-right and choose *Create – Bus* from the pop-up menu |
| Delete a bus | Select a bus, then choose *Objects – Delete*  
  - or -  
  Select a bus, then press *Delete* |
| Rename a bus | Select a bus, then choose *Objects – Rename*  
  - or -  
  Select a bus, then click-right and choose *Rename* from the pop-up menu |
| Create an ECSet based on an existing bus | Select a bus, then choose *Objects – Create – Electrical CSet*  
  - or -  
  Select a bus, then click-right and choose *Create – Electrical CSet* from the pop-up menu |
| Select/Deselect a bus in Allegro or SPECCTRAQuest | Select a bus, then choose *Objects – Select* (or Deselect)  
  - or -  
  Select a bus, then click-right and choose *Select* (or Deselect) from the pop-up menu |
A bus is created by selecting net or Xnet objects in the appropriate worksheet and then choosing *Objects – Create Bus.* Figure 2-5 shows the Create Bus dialog box.

**Figure 2-5 Create Bus dialog box**

![Create Bus dialog box](image)
The nets and Xnets that make up a bus can be changed by selecting a bus and then choosing *Objects – Bus Membership*. Figure 2-6 shows the Bus Membership dialog box.

**Figure 2-6 Bus Membership dialog box**

![Bus Membership dialog box]

**Working with Match Groups**

Groups are a collection of nets, Xnets, or pin-pairs which must all match or be relative to a specific target within the group.

If a delta value is not defined, all members of the group will be matched within the specified tolerance. If a delta value is defined, then all members of the group will be relative to a specific target net.

See “Relative/Matched Group” on page 24 for more information on Relative/Match group objects.

You can define a generic group for an ECSSet. The generic group will be used to automatically define the net- or Xnet-specific groups when the ECSSet is referenced.

See Chapter 3, “Working With Constraints” for information about creating ECSSets and associating them with objects.
Relative/Match Group Rules

The following rules apply to Relative/Match Groups

- A Match Group can only be specified in Relative Propagation Delay worksheet of the Routing workbook.
- Relative/Match group constraints can be set for the entire group; individual members of the group can have overrides offering differing levels of tolerance as desired.
- Relative/match group delays can be defined at the design level or at the system level.
- A match delay constraint from pre-14.0 board database will be upreved with a delta value of zero. This implies that all group members will match a specified target pin-pair.

**Note**: Constraint Manager, when launched from Allegro Designer, supports match groups only at the net level, not at the pin-pair level.

See “Relative/Matched Group” on page 24 for more information on Relative/Match group objects.

Operations on a Match Group

This section summarizes match group operations. Refer to the online help for detailed instructions.

**Table 2-4 Operations on a match group**

<table>
<thead>
<tr>
<th>Operation</th>
<th>Command</th>
</tr>
</thead>
<tbody>
<tr>
<td>Create a match group</td>
<td>- Select a net, Xnet, or pin-pair in the Relative Propagation Delay worksheet, then choose Objects – Create – Match Group</td>
</tr>
<tr>
<td></td>
<td>- or –</td>
</tr>
<tr>
<td></td>
<td>- Select a net, Xnet, or pin-pair, then click-right and choose Create – Match Group from the pop-up menu</td>
</tr>
<tr>
<td>Delete a match group</td>
<td>- Select a match group, then choose Objects – Delete – or –</td>
</tr>
<tr>
<td></td>
<td>- Select a match group, then press Delete</td>
</tr>
<tr>
<td>Operation</td>
<td>Command</td>
</tr>
<tr>
<td>---------------------------------</td>
<td>-------------------------------------------------------------------------</td>
</tr>
<tr>
<td>Rename a match group</td>
<td>- Select a match group, then choose <em>Objects – Rename</em> – or –</td>
</tr>
<tr>
<td></td>
<td>- Select a match group, then click-right and choose <em>Rename</em> from the pop-up menu</td>
</tr>
<tr>
<td>Select/Deselect a match group</td>
<td>- Select a match group, then choose <em>Objects – Select (or Deselect)</em> – or –</td>
</tr>
<tr>
<td>in Allegro or SPECCTRAQuest</td>
<td>- Select a match group, then click-right and choose <em>Select (or Deselect)</em> from the pop-up menu</td>
</tr>
<tr>
<td>Examine match group membership</td>
<td>- Select a match group, then choose <em>Objects – Match Group Membership</em> – or –</td>
</tr>
<tr>
<td></td>
<td>- Select a match group, then click-right and choose <em>Match Group Membership</em> from the pop-up menu – or –</td>
</tr>
<tr>
<td></td>
<td>- Select a match group, then click-right and choose <em>Expand</em> from the pop-up menu</td>
</tr>
<tr>
<td>Redefine members of a match group</td>
<td>- Select a match group, then choose <em>Objects – Match Group Membership</em> – or –</td>
</tr>
<tr>
<td></td>
<td>- Select a match group, then click-right and choose <em>Match Group Membership</em> from the pop-up menu – or –</td>
</tr>
<tr>
<td></td>
<td>- Select a match group member, then click-right and choose <em>Remove</em> from the pop-up menu</td>
</tr>
</tbody>
</table>
A match group is created by selecting objects in the Relative Propagation Delay worksheet of the Routing workbook and then choosing *Objects – Create Match Group*. Figure 2-7 shows the Create Match Group dialog box.

**Figure 2-7 Create Match Group dialog box**

![Create Match Group dialog box](image)

The members that make up a match group can be changed by selecting a match group and then choosing *Objects – Match Group Membership*. Figure 2-8 shows the Match Group Membership dialog box.

**Figure 2-8 Match Group Membership dialog box**

![Match Group Membership dialog box](image)
Working With Constraints

Topics in this chapter include

- **Electrical Constraint Sets** on page 42
- **Working with ECSets** on page 45
- **Operations on ECSets** on page 47
Electrical Constraint Sets

An electrical constraint set (ECSet) is a collection of constraints, and their default values, which reflect a particular design requirement. You can capture any, or all, electrical constraints, including topology-related information, in an ECSet.

When you access an ECSet worksheet, the following objects are presented hierarchically. The System is the top-most object with pin-pairs at the bottom of the hierarchy with the highest precedence.

**Note:** Constraint Manager, when launched from Allegro Designer, does not support the Signal Integrity and Timing workbooks.

**Figure 3-1 Electrical Constraint Set Folder Object Hierarchy**

ECSets reside in the Electrical Constraint Set object folder

Design objects reside in Net object folder

The *Signal Integrity* worksheet at the Electrical Constraint Set-level depicted in Figure 3-1 shows the following objects and ECSets:

<table>
<thead>
<tr>
<th>System</th>
<th>BOARD_2_BCKPLN</th>
</tr>
</thead>
<tbody>
<tr>
<td>Designs</td>
<td>B_1, B_2, B_3</td>
</tr>
<tr>
<td>Electrical</td>
<td>MEM_CNTRL_CSET, PCI_CSET, TTL_CSET,</td>
</tr>
<tr>
<td>CSets</td>
<td>VIDEO_DATA_CSET</td>
</tr>
</tbody>
</table>

You define generic rules, such as ECSets, under the *Electrical Constraint Set* object folder. These generic rules can subsequently be applied to net-related objects.
As design requirements change, you can

- Edit the ECSet constraints. All net-related objects that reference the ECSet will automatically inherit these changes.
- Assign a different ECSet, one that reflects a different rule-set, to the net-related object.
- Define override properties on individual net-related objects.

You can also define an ECSet based on the characteristics of a net or Xnet. Defining net-derived rules lets you create (or clone) rules based on the electrical characteristics of the physical net in your design.

**Referencing ECSets**

When an ECSet is referenced from a net-related object, certain constraints are inherited while others are actually applied to the objects. For example, topology information must be applied and cannot be simply inherited due to the mapping that must occur between the ECSet and the net objects.

**Important**

When you click in a worksheet cell, the source of the information, the ECSet name if inherited, appears in the status bar.

When an ECSet is updated from importing a topology template, the characteristics of the net-related objects must match those of the topology template. Otherwise, the referenced ECSet in Constraint Manager will not be refreshed with this new constraint information.

➤ Choose Audit – Constraints to view a report of constraints that have net-related overrides.

➤ Choose Audit – Electrical CSets to view a report of all objects referenced by each ECSet.

See Chapter 4, “ECSets and Topology Templates” for information about topology templates and how they relate to ECSets.

**Note:** Constraint Manager, when launched from Allegro Designer, does not support topology templates.
ECSet Rules

The following rules apply to ECSets:

- All ECSets are presented under the appropriate Design or System and can be referenced only by objects within the same Design or System.
- ECSets can be referenced by any number of net-related objects (bus, diff pair, Xnet, or net) but an object may reference only one ECSet.
- You cannot delete an ECSet without first removing all net-type object references to the ECSet.
Working with ECSets

➤ Create an ECSet

- **Drop-down Menu Pick**
  - Objects
    - Exit
    - Highlight
    - Dehighlight
    - Expand
    - Collapse
    - Bus Membership
    - Match Group Membership
    - Remove
  - Create
    - Rename
    - Delete
    - Electrical CSet References
    - Report
- **Context Menu Pick (click-right)**
  - Analyze
    - Highlight
    - Dehighlight
    - Expand
    - Collapse
    - Match Group Membership
    - Remove
    - Create
    - Rename
    - Delete
    - Electrical CSet References
    - SigXplorer

Clean ECSet yields (no ECSet or net-related object)

Cloned ECSet yields (ECSets or net-related object selected)
➤ Assign ECSet to net-related object

Select Net-Related Design

Choose from the available ECSets
Operations on ECSets

This section summarizes ECSet operations. Refer to the online help for detailed, step-by-step instructions.

Table 3-1 Operations on a ECsets

<table>
<thead>
<tr>
<th>Operation</th>
<th>Command</th>
</tr>
</thead>
</table>
| Create an empty ECSet      | - In the Electrical Constraint Set object folder, click on a workbook, or a worksheet within a workbook, then choose Objects – Create – Electrical CSet.  
|                            | - or –                                                                  |
|                            | - In the Electrical Constraint Set object folder, click on a workbook, or a worksheet within a workbook, then click on an existing ECSet, and choose Objects – Create – Electrical CSet (or click-right and choose Create – Electrical CSet from the pop-up menu).  
|                            | Make sure you deselect the copy constraints from checkbox.           |
|                            | - or –                                                                  |
|                            | - In the Nets object folder, click on a workbook followed by a worksheet, then click on the desired net, Xnet, bus, or pin-pair and choose Objects – Create – Electrical CSet (or click-right and choose Create – Electrical CSet from the pop-up menu).  
|                            | Make sure you deselect the copy constraints from checkbox.           |

Important

Once the ECSet has been created, you specify constraint parameters in a worksheet cell of the ECSet. It may be helpful to click-right and choose Change from the pop-up menu. This will guide you through the appropriate parameters and syntax that applies for the specific constraint type that the cell represents.
Operation | Command
---|---
Clone an ECSet | In the Electrical Constraint Set object folder, click on a workbook, or a worksheet within a workbook, then click on an existing ECSet, and choose *Objects – Create – Electrical CSet* (or click-right and choose *Create – Electrical CSet* from the pop-up menu).

Make sure you select the *copy constraints from* checkbox.

– or –

In the Nets object folder, click on a workbook followed by a worksheet, then click on the desired net, Xnet, bus, or pin-pair and choose *Objects – Create – Electrical CSet* (or click-right and choose *Create – Electrical CSet* from the pop-up menu).

Make sure you select the *copy constraints from* checkbox.

Associate a design object with an ECSet | In the Electrical CSet object folder, click on the desired ECSet and choose *Objects – Electrical CSet References* (or click-right and choose *Electrical CSet References* from the pop-up menu), then choose the appropriate design object (net, Xnet, bus, or diff pair) from the drop-down menu, then move the desired target objects into the *references* column.

– or –

In the Nets object folder, click on the desired design object (net, Xnet, bus, or diff pair), then choose *Objects – Electrical CSet References* (or click-right and choose *Electrical CSet References* from the pop-up menu), then move the desired target objects into the *references* column.
**Operation**  
Examine objects reference by an ECSet  
- In the Electrical CSet object folder, click on a workbook, or a worksheet within a workbook, then click on an existing ECSet and choose *Objects – Electrical CSet References* (or click-right and choose *Electrical CSet References* from the pop-up menu)

Next choose the appropriate design object (net, Xnet, bus, or diff pair) from the drop-down menu.

The referenced objects will appear in the *references* column.

Examine the ECSet referenced by an object  
- In the Nets object folder, click on a workbook, or a worksheet within a workbook, then click on an existing design object (net, Xnet, bus, or diff pair) and choose *Objects – Electrical CSet References* (or click-right and choose *Electrical CSet References* from the pop-up menu)

- or –  

- Note the ECSet adjacent to the selected design object (net, Xnet, bus, or diff pair) in the *Referenced Electrical CSet* column.

**Note:** When you click in a worksheet cell, the source of the information, the ECSet name if inherited, appears in the status bar.

Delete an ECSet  
Before you can delete an ECSet, the ECSet must not be referenced by any design objects. Select the design object, then choose *Objects – Electrical Cset References*.

- In Electrical Constraint Set object folder, click on an ECSet, then choose *Objects – Delete*.

- or –

- In Electrical Constraint Set object folder, click on an ECSet, then press *Delete*.  

**Command**
Operation

Rename an ECSet

Command

- Select an ECSet, then choose Objects – Rename (or click-right and choose Rename from the pop-up menu).
ECSets and Topology Templates

Topics in this chapter include

- “What is a Topology Template?” on page 52
- “Importing ECSets” on page 54
- “Mapping Templates and ECSets to Net-related Objects” on page 56
- “Auditing ECSets” on page 59
- “Exporting ECSets” on page 64
- “Migrating Pre 14.0 Electrical Rule Sets” on page 64
What is a Topology Template?

A topology template file (.top) is an on-disk image of the SigXplorer database. A topology template file contains the same data as an ECSet, including electrical constraints, but it also contains information to support the graphical representation of a circuit topology in SigXplorer.

**Note:** Constraint Manager, when launched from Allegro Designer, does not support topology exploration. If you are using Allegro Designer, you can ignore the descriptions of the following commands in this chapter:

- *File – Import Electrical CSets*
- *File – Import Analysis Results*
- *File – Export Electrical CSets*
- *File – Export Analysis Results*
- *Audit – Topology Templates*

In pre-14.0 designs, a topology template was applied to a group of target nets. In the process, constraint information was extracted from the topology file and flattened; constraints were copied to individual target nets as properties. With Constraint Manager, these properties are not flattened; they remain intact, collectively, as an ECSet. Net-related objects in the design reference the ECSet rather than a collection of individual properties.

The topology template can be imported to, and exported from, Constraint Manager. When imported, the topology template information will be instantiated within Constraint Manager as an ECSet where it can be manipulated separate from the topology template. The ECSet is saved with the database of the host application from which Constraint Manager was invoked: a board file (.brd) or a schematic view.
With such a close alignment between a topology template and an ECSet, SigXplorer can be accessed directly from Constraint Manager. In fact, you can define your constraints in SigXplorer—as a topology template—and then import this information into Constraint Manager as an ECSet. Conversely, you can define your constraints in Constraint Manager—as an ECSet—and then export this information to SigXplorer as a topology template. See the Design Exploration Phase (with SigXplorer) on page 95 for information on the Constraint Manager-SigXplorer design flow.

The only constraint that you cannot define in Constraint Manager is user-defined pin scheduling. This must be defined in SigXplorer. You can, however, select from a list or pre-defined pin schedules in Constraint Manager.
Importing ECSets

Constraint Manager promotes design reuse through the following commands:

<table>
<thead>
<tr>
<th>Use this command</th>
<th>To</th>
</tr>
</thead>
<tbody>
<tr>
<td>File – Import – Electrical CSets</td>
<td>Import a selected on-disk topology template into Constraint Manager. The imported template will become an ECSet which can be referenced by net-related objects that share the same electrical characteristics. See “Mapping Templates and ECSets to Net-related Objects” on page 56. If the imported template was previously assigned as an ECset, the import will overwrite existing constraint values. Note: If the Automatic Topology Update checkbox is enabled (Tools – Options Figure 4-2 on page 57), the refreshed template information is immediately applied to the net-related objects; otherwise, you must choose Tools – Update Topology to apply the changes.</td>
</tr>
</tbody>
</table>
Use this command | To
---|---
File – Import – Constraints | Import the dictionary and constraints file (.DCF) archived on disk. The dictionary and constraints file is a snapshot of electrical constraint information. It may include any user-defined properties, ECSets and their constraints, and net-related objects and their constraints (including ECSet references).

**Note:** If you are using Constraint Manager, when launched from Allegro Designer, and you import constraints from a board designed with Allegro Expert, choosing *Overwrite current constraints, Merge current constraints, or Replace current constraints* will affect constraints in the Routing workbook only; constraints that may exist in the Signal Integrity and Timing workbooks will remain unchanged.

You can choose from the following options when importing constraints.

**Overwrite current constraints**

- Erases current constraints and reads in new constraints.
- Generates a report of the import.

**Merge with existing constraints**

- Preserves current constraints and reads in new constraints.
- Generates a report of the import.

**Replace current constraints**

- Overwrites only those objects which are constrained in the DCF file being imported.

**Report only**

- Generates a report of the import (*Overwrite or Merge*) without executing the import.
Mapping Templates and ECSets to Net-related Objects

Allegro, SPECCTRAQuest, and APD can intelligently map the constraint information, imported from a topology template or defined in an ECSet, to a candidate net that matches the topological characteristics of the referenced ECSet. If the candidate net does not match these topological characteristics, the mapping will fail and the constraints will not be applied.

The following will result in a mismatch:

- A traces or via element in the topology; only T lines can connect components
- A terminator connected to multiple pins on a component
- More than one terminator on a node
- More than one component pin connected to a node; T lines must separate component pins
- A voltage source that is not connected to a discrete component
- Any disconnected components
- Sweepable ranges on discrete components; only a single value is allowed

**Note:** When Constraint Manager is running with Concept HDL, the topological constraints are not applied. Topological mapping will occur when the constraint information is fed-forward to the design. See the Design Capture Phase (with Concept HDL) on page 97 for information on the Constraint Manager-Concept HDL design flow.

Mapping ensures that the templates be applied to a class of nets which can accept the desired schedule and pin-pair constraints.

The following comparisons are used when mapping an ECSet to a referenced candidate net.

- Driver pins
- Receiver pins
- Input/Output pins
- Connector pins
- Discrete pins

The comparison considers the number of pins and their direction (pinuse property) and reference designators. If the mapping is successful, constraints will be inherited from the ECSet as follows:
Pin-pairs with switch/settle constraints will appear as children of the Xnet or Net in the Switch/Settle Delays worksheet of the Timing workbook.

Pin-pairs with propagation constraints will appear as children of the Xnet or Net in the Min/Max Propagation Delays worksheet of the Routing workbook.

Pin-pairs with impedance constraints will appear as children of the Xnet or Net in the Impedance worksheet of the Routing workbook.

Match Groups will appear in the Relative Propagation Delays worksheet of the Routing workbook.

The schedule constraint will be populated in the Wiring Worksheet of the Routing workbook.

All other electrical constraints will be inherited regardless if the mapping is successful since the other constraints are not topology specific.

Choose Tools—Options to control how objects in Constraint Manager inherit constraint information.

**Figure 4-2 Options Dialog Box with Default Settings**

The following describes how to use the Electrical CSet Apply fields of the Options dialog box (see Figure 4-2 on page 57).
### Constraint Manager Design Guide

**ECSets and Topology Templates**

**Checkbox Option** | **Function**
--- | ---
**Automatic topology update** | Controls how topology-related constraints are re-applied
- When the design changes (component placement, signal model updates)
  - or -
- When an ECSet is initially referenced
When *enabled*, changes are applied on-the-fly as the design changes.
When *disabled*, changes must be applied by choosing *Tools—Update Topology*.

**Note:** Disabling automatic topology update may be necessary when design changes are frequent and complex ECSets are referenced.

- **Rip up etch when mapping topology**

- **Overwrite existing constraints**

### Important

Enabling ‘overwrite existing constraints’ is necessary when migrating pre-14.0 designs using the *Audit — Topology Properties* command. This will ensure that all net-related overrides—created by the pre-14.0 topology template mapping software—are removed.
Auditing ECSets

Constraint Manager provides audits to give you feedback, in report form, about the constraints, and their references, used in the design. Audit commands are available when Constraint Manager is invoked from SPECCTRAQuest, Allegro, APD, or Concept HDL. The following audits (accessed from the Audit menu) relate to ECSets.

<table>
<thead>
<tr>
<th>Run this audit</th>
<th>To</th>
</tr>
</thead>
<tbody>
<tr>
<td>Constraints</td>
<td>List net-related overrides and constraint violations.</td>
</tr>
<tr>
<td>Obsolete Objects</td>
<td>List objects that should, but no longer exist in the Allegro or Concept HDL database, yet they are still being referenced in Constraint Manager.</td>
</tr>
<tr>
<td>Electrical CSets</td>
<td>List the mapping status of all objects which reference ECSets.</td>
</tr>
<tr>
<td>Topology Properties</td>
<td>Migrate ASSIGN_TOPOLOGY and TOPOLOGY_TEMPLATE properties to an ECSet reference.</td>
</tr>
</tbody>
</table>

**Note:** Constraint Manager, when launched from Allegro Designer, does not support pin-pairs. Any pin-pairs that exist will appear as ‘not supported’ in the audit report.

The sections that follow describe these audits.

**Constraint Audit**

The Constraints audit (*Audit – Constraints*) generates a report listing constraint errors. This report will aid you in troubleshooting constraint violations. The audit includes the following checks:

- Min values that exceed Max values
- Values less than zero
- Completeness violations
Constraint Manager Design Guide
ECSets and Topology Templates

- Group membership violations
- Relative group violations
- Paired parallelism lengths and gap
- Setup and hold relative to clock period
- Net-related overrides

Obsolete Objects Audit

The Obsolete Objects audit (Audit – Obsolete Objects) generates a report that lists objects that must be reconciled between Constraint Manager and the Allegro- or Concept HDL databases. Constraint Manager will display a No Obsolete Objects message as appropriate.

For example, if you use Constraint Manager to constrain an object in Concept HDL, that object will be stored in Concept HDL's constraint view of the HDL library. If you later delete that object in Concept HDL, that constraint will still be in Constraint Manager until it is reconciled with the obsolete objects audit.

This command is used subsequent to importing a dictionary and constraint file (File – Import – Constraints) or when the connectivity is disjoint between the component or net in Concept HDL and the corresponding Constraint Manager object.

Note: The Audit – Obsolete Objects command is not available when running Constraint Manager in stand-alone mode.

The Audit Obsolete Objects dialog box contains the following fields:

Table 4-1  Obsolete Objects Dialog Box Options

<table>
<thead>
<tr>
<th>Use this field</th>
<th>To</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type</td>
<td>Filter on an object type (bus, net, Xnet)</td>
</tr>
<tr>
<td>Obsolete Objects</td>
<td>List all objects that no longer exist in the Allegro or Concept HDL database, yet exist in Constraint Manager</td>
</tr>
<tr>
<td>Existing Objects</td>
<td>List all objects that exist in the Allegro or Concept HDL database, and in Constraint Manager</td>
</tr>
<tr>
<td>Delete</td>
<td>Remove objects, listed in the obsolete objects list, from the Allegro or Concept HDL database.</td>
</tr>
</tbody>
</table>
Electrical CSets Audit

The Electrical CSets audit (Audit – Electrical CSets) generates a report listing the current ECSets in the design and the status of all net-related objects that reference them.

The status reports the inheritance for each constraint defined in the ECSet including:

- Any mismatch of the topological characteristics between a net-related object and the ECSet (in which case, the constraint from the ECSet is not inherited).
- The net-related object that inherits the ECSet constraint.

Topology Templates Audit

The Topology Templates audit (Audit – Topology Templates) migrates deprecated properties to ECSet references used by Constraint Manager.

**Note:** Constraint Manager, when launched from Allegro Designer, does not support topology templates.

In pre-14.0 designs, electrical constraints were captured using three entities: the topology template (specified with the TOPOLOGY_TEMPLATE property), the topology assignment (specified with the ASSIGN_TOPOLOGY property), and the constraint set (specified with the ELECTRICAL_CONSTRAINT_SET property).
In 14.0 designs, only the ECSet association is supported; the `TOPOLOGY_TEMPLATE` and the `ASSIGN_TOPOLOGY` properties are no longer required. All topology information is now contained in the ECSet (specified with the `ELECTRICAL_CONSTRAINT_SET` property).

The topology templates audit removes the `TOPOLOGY_TEMPLATE`, `TOPOLOGY_TEMPLATE_REVISION`, and `ASSIGN_TOPOLOGY` references from net-related objects.

The Audit Topology Templates dialog box contains the following fields:

**Table 4-2 Audit Old Template Dialog Box Options**

<table>
<thead>
<tr>
<th>Use this field</th>
<th>To</th>
</tr>
</thead>
<tbody>
<tr>
<td>Topology template values (drop-down menu)</td>
<td>List all <code>TOPOLOGY_TEMPLATE</code> and <code>ASSIGN_TOPOLOGY</code> property values in the design.</td>
</tr>
<tr>
<td></td>
<td>Once a property value is selected from the drop-down menu, all nets which have the same template value will be listed.</td>
</tr>
</tbody>
</table>

**Update to use Electrical Cset . . .**

- **Import (radio button)**
  - Import a new template. The field beside the radio button will be populated with a Topology Template (.top file) name if one can be found on disk.
  - Constraint Manager uses the `TOPOLOGY_TEMPLATE_PATH` environment variable to search for a template file with the same name as the property value

- **Browse**
  - Find the appropriate template file if Constraint Manager cannot locate it.

- **Existing (radio button)**
  - Use an existing ECSet. This option will be the default if the design contains an ECSet with the same name as the property value
## Constraint Manager Design Guide

### ECSets and Topology Templates

<table>
<thead>
<tr>
<th>Use this field</th>
<th>To</th>
</tr>
</thead>
<tbody>
<tr>
<td>Overwrite existing constraints (check box)</td>
<td>Controls whether constraint values in the ECSets will overwrite any existing net-related constraints when an ECSet is re-applied.</td>
</tr>
</tbody>
</table>

**Important**

Enabling ‘overwrite existing constraints’ is necessary when migrating pre-14.0 designs. This will ensure that all net-related overrides—created by the pre-14.0 topology template mapping software—get removed.

Apply | Migrate all listed nets to reference the imported or existing ECSets. Once migrated, nets will have their TOPOLOGY_TEMPLATE and ASSIGN_TOPOLOGY properties deleted. Constraint Manager displays a properties up to date message as appropriate.
Exporting ECSets

Constraint Manager promotes design reuse through the following commands:

<table>
<thead>
<tr>
<th>Use this command</th>
<th>To</th>
</tr>
</thead>
<tbody>
<tr>
<td>File – Export – Electrical CSets</td>
<td>Save selected ECSets, from a design, or from a system, to a topology template (.top) file on disk.</td>
</tr>
</tbody>
</table>

File – Export – Constraints

Export a dictionary and constraints file (.dcf) to disk. The dictionary and constraints file contains a complete snapshot of all electrical constraint information. This includes any user-defined properties, all ECSets and their constraints, and all net-related objects and their constraints (including ECSet references).

You would typically save to a dictionary and constraint file prior to making extensive constraint modifications within Constraint Manager. The dictionary and constraints file would then be considered an archive from which you could revert back.

Exporting a dictionary and constraints file results in overwriting constraint data saved from a previous archive.

Migrating Pre 14.0 Electrical Rule Sets

Designs created prior to release 14.0 may contain Electrical Rule Sets. As part of the process of upreving a design to release 14.0, these Electrical Rule Sets are migrated to Constraint Manager as Electrical Constraint Sets (ECSets). See Appendix A for details.
Constraint Analysis

Topics in this chapter include

- “Viewing Worksheet Cells and Objects” on page 69
- “Analyzing for Rule-based Constraints” on page 72
- “Analyzing for Simulation-based Constraints” on page 75
- “Analyzing with Custom Measurements and Custom Stimulus” on page 79
- “Analysis Results” on page 87
- “Interpreting Analysis Results Returned to a Worksheet” on page 89
- “Constraints Across the System” on page 92
How Constraint Manager Performs Analysis

Constraint Manager analyzes the constraints in your design using two methods:

- **Design Rule Checks**

  Real-time design rule checks are made on objects constrained in the *routing* worksheets. Results are returned to the worksheet cells in focus by comparing changes in the layout, such as moving a part, against the constraint limits that you specified for these objects.

  As design rule violations are encountered, Constraint Manager colors the corresponding worksheets cells in red. Additionally, bow tie markers appear on offending objects in the layout.

  See “Analyzing for Rule-based Constraints” on page 72 for information about interactive, online design rule checking.

- **Simulated Analysis**

  Simulated analysis is made on objects constrained in the *signal integrity* and *timing* worksheets.

  **Note:** Constraint Manager, when launched from Allegro Designer, does not support the *signal integrity* and *timing* workbooks.

  Analyzed results are returned to the worksheet cells in focus by comparing computations (the actual) against the constraint limits that you specified for these objects. The actual, and the difference between the actual and the set constraint limit (the margin) are returned.

  See “Analyzing for Simulation-based Constraints” on page 75 for information about analyzed constraints.

  **Note:** Constraint Manager uses the same color scheme for both analyzed results and design rule checks. See “Cell Colors used in Analysis” on page 67 for more information.

**Important**

You can click on an object in a Constraint Manager worksheet and choose *Object* – *Select* to highlight that object in the layout.
Cell Colors used in Analysis

In addition to controlling many of the user interface elements employed in Constraint Manager (View – Options), you can modify the cell colors used when returning results from analysis.

Figure 5-1  Modifying cell colors

The analysis engine computes a value (actual) and compares this to the value specified in the ECSet. The difference between the analysis value and the specified constraint value is the margin. Both actuals and margins are returned to the cells in the appropriate worksheets.

You use the following options to control cell colors.

<table>
<thead>
<tr>
<th>Use this field</th>
<th>To</th>
</tr>
</thead>
<tbody>
<tr>
<td>Color Legend</td>
<td>Display the colors palette. Once displayed, you can selectively display or hide the cell color options (pass, fail, analysis error, directly set).</td>
</tr>
<tr>
<td>Pass</td>
<td>Specify the cell color for resulting analysis values (actuals) that meet the specified constraint setting.</td>
</tr>
<tr>
<td>Fail</td>
<td>Specify the cell color for resulting analysis values (actuals) that do not meet the specified constraint setting.</td>
</tr>
</tbody>
</table>
### Analysis error

Specify the cell color when analysis cannot be performed. The *status* window displays the cause of the error.

Possible failures may result from trying to analyze with:

- *only* Concept HDL and Constraint Manager running. Allegro/APD or SPECCTRAQuest must be running to access the analysis engine.
- Unplaced components
- Unrouted nets (on stub length and impedance checks)
- Incorrect (or missing) signal models
- Missing trace information
- Inactive DRC mode (see “Analysis Results” on page 87).

### Directly set

Specify the cell color of an ECSets assignment or a net-related constraint override set on an object.

### Use defaults

Restore the default cell color scheme:

- **Pass** = green
- **Fail** = red
- **Analysis error** = yellow
- **Directly set** = blue

If you have modified color options (pass, fail, analysis error, directly set), these settings will be recalled when you uncheck *use defaults*.

### Use colors

Turn off cell colors.

At times, it may be easier on your eyes to examine cells without colors. Simply uncheck the *use colors* checkbox to turn off cell colors.
Main Window

Increase the available screen area for viewing the worksheets. You can hide the tool bar, status bar, worksheet selector, and color legend. Alternatively, you can un-dock, and reposition, the color legend.

**Caution**

*The status bar provides key feedback on many operations. We recommend that you do not hide it.*

### Viewing Worksheet Cells and Objects

As the complexity of your design increases, the number of objects in your design increases; and, correspondingly, the number of ECSets associated with those objects increases. This can lead to a high-level of congestion in your worksheets. Fortunately, Constraint Manager lets you easily change your view of constraints, letting you change your focus as you work.

Refer to the *Common worksheet commands* table on page 70 for commands that aid you in manipulating worksheets.
### Table 5-1 Common worksheet commands

<table>
<thead>
<tr>
<th>Task</th>
<th>Related Commands</th>
<th>Actions</th>
</tr>
</thead>
</table>
| Locate an object, a result, or an ECSSet | **Edit – Find** | Sequences through each occurrence of the specified object. You can filter on the following:  
  - design  
  - net  
  - Xnet  
  - pin-pair  
  - result  
  - diff pair  
  - bus  
  - match group  
  - ECSSet |
|  | **Edit – Go to source** | Locates the parent object that owns the inherited ECSSet of the selected child object. For example, if you select a child object, such as a bit in a bus, its constraints are most-likely inherited from an ECSSet that is associated with the parent object, in this case the bus. |
|  | **View – Options – Row Numbers** | Enable row numbering in the worksheets. |
|  | **Objects – Filter** | Selectively display (or hide) objects in the worksheets. You can filter on the following:  
  - net  
  - Xnet  
  - diff pair  
  - bus |
<table>
<thead>
<tr>
<th>Task</th>
<th>Related Commands</th>
<th>Actions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Control the worksheet or object hierarchy</td>
<td><em>Objects – Expand/Collapse</em></td>
<td>Expand or collapse the worksheet hierarchy in the worksheet selector or the object hierarchy in the worksheets. Worst-case analysis results on collapsed (hidden) objects are rolled up to the expanded object. This notification lets you work at any level in the object hierarchy.</td>
</tr>
<tr>
<td>Work in columns</td>
<td><em>Column – Sort</em> (or double-click the column head)</td>
<td>Reverse the ordering of objects or constraint values in a column.</td>
</tr>
<tr>
<td>Work in columns</td>
<td><em>View – Hide/Show Column</em></td>
<td>Hide columns in a worksheet so you can focus on a single, or a few, columns. Otherwise, you may have to scroll horizontally to access an out-of-view column.</td>
</tr>
<tr>
<td>Compare cells</td>
<td><em>Window – Tile</em></td>
<td>Compare the cells of two or more different worksheets. You may have to scroll to view the desired cells.</td>
</tr>
<tr>
<td>Compare cells</td>
<td><em>Window – New Window</em></td>
<td>Compare cells in the same worksheet. Constraint Manager opens the same worksheet in a different window. This lets you scroll to different cell views while allowing you to make concurrent edits in the same worksheet.</td>
</tr>
</tbody>
</table>
Analyzing for Rule-based Constraints

Constraint Manager has three modes of design rule checking. You control design rule checks with the DRC tab of the Analysis Modes dialog box (Analyze – Analysis Modes). Alternatively, you can specify analysis settings, DRC modes, and desired reports from a single dialog box (Objects – Report).

**Note:** Constraint Manager, when launched from Allegro Designer, does not support custom measurements or custom stimulus; therefore, only the DRC modes tab is visible in the Analysis Modes dialog box. Furthermore, the Max xtalk and Max peak xtalk DRC fields are hidden.

**Figure 5-2 Analysis Modes dialog box:** DRC view

- Refer to the DRC Constraint Modes table on page 73 for information about how to use DRC constraint modes.
- Refer to the Online Design Rule Checks table on page 74 for information about the online design rule checks made in Constraint Manager.
# Table 5-2 DRC Constraint Modes

<table>
<thead>
<tr>
<th>Use this constraint mode</th>
<th>To</th>
</tr>
</thead>
<tbody>
<tr>
<td>All On</td>
<td>Interactively check for design rule violations.</td>
</tr>
<tr>
<td></td>
<td>- Design rule violations will appear in the appropriate worksheet cell in <em>red</em> for all objects that have offending constraints in an assigned ECSet.</td>
</tr>
<tr>
<td></td>
<td>- Design rule violations will appear in reports (<em>Object – Report</em>).</td>
</tr>
<tr>
<td></td>
<td>- A DRC bowtie marker will appear in the Allegro/APD or SPECCTRAQuest layout.</td>
</tr>
<tr>
<td></td>
<td>Uncheck the <em>On-line DRC checkbox</em> to temporarily disable interactive design rule checks. This is useful when you need to make compute-intensive placement or routing modifications and you don’t want to hinder system performance.</td>
</tr>
<tr>
<td>All Off</td>
<td>Disable design rule checking to improve system performance.</td>
</tr>
<tr>
<td>All Batch</td>
<td>Check for design rule violations <em>only</em> when a batch command (such as <code>drc update</code> or <code>dbfix</code>) is performed in Allegro/APD or SPECCTRAQuest.</td>
</tr>
</tbody>
</table>

*Important*

When you turn DRC back on (check the *On-line DRC checkbox*), the constraint status is stale; you must analyze in Constraint Manager or specify a DRC update in Allegro/APD or SPECCTRAQuest to refresh the design rule checks.
### Table 5-3 Online Design Rule Checks

<table>
<thead>
<tr>
<th>Constraint Name</th>
<th>DRC Computation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Stub length</td>
<td>Compares each segment of an extended net for a stub length that exceeds the specified constraint value.</td>
</tr>
<tr>
<td>Net schedule</td>
<td>Compares the clines in an extended net with the ratsnest lines. Any mismatch generates a violation.</td>
</tr>
<tr>
<td>Max via count</td>
<td>Totals the number of vias in an extended net and compares this to the specified constraint value.</td>
</tr>
<tr>
<td>Max exposed length</td>
<td>Totals the exposed cline length in an extended net and compares this to the specified constraint value. Exposed etch includes clines which are not protected by power and ground planes.</td>
</tr>
<tr>
<td>Propagation delay</td>
<td>Compares the delay or length of a specific pin-pair against a specified min/max constraint value.</td>
</tr>
<tr>
<td>Relative propagation delay</td>
<td>Compares the difference in delay or length among a group of two or more pin-pairs.</td>
</tr>
<tr>
<td>Max parallel</td>
<td>Specifies the total length of parallel clines that are allowed on an extended net for a specified separation.</td>
</tr>
<tr>
<td>Impedance</td>
<td>Compares the impedance of each cline segment of an extended net to the specified constraint value.</td>
</tr>
<tr>
<td>Max xtalk</td>
<td>Specifies the total amount of crosstalk that is allowed on an extended net from all other extended nets in the design. <strong>Note:</strong> Not supported when Constraint Manager is launched from Allegro Designer.</td>
</tr>
<tr>
<td>Max peak xtalk</td>
<td>Specifies the total amount of crosstalk that is allowed on an extended net from any other extended net in the design. <strong>Note:</strong> Not supported when Constraint Manager is launched from Allegro Designer.</td>
</tr>
</tbody>
</table>
Analyzing for Simulation-based Constraints

Certain constraints (signal integrity and timing) require simulation to compute actual values. When the actual value is analyzed and returned to a worksheet cell, it is compared with the specified constraint value that is associated with the object being analyzed. The difference is calculated and displayed in the margin column.

Important

To analyze for simulation-based constraints, Constraint Manager must be run with Allegro, APD or SPECCTRAQuest.

Before you initiate an analysis (Analyze – Analyze) on an object, you should configure the analysis engine (Analyze – Settings). Alternatively, you can specify analysis settings, DRC modes, and desired reports from a single dialog box (Objects – Report).
In the Analysis Settings dialog box, you specify the type of simulation, whether to use crosstalk timing windows, and the type of stimulus.

You can click Preferences to specify buffer information (in the Analysis Preferences dialog box). You can also choose to save a waveform for each analysis; waveforms can subsequently be viewed in SigWave (Tools – SigWave).

See the SPECCTRAQuest Simulation and Analysis Reference for detailed information on analysis settings and preferences.

**Custom Measurements and Custom Stimulus**

Constraint Manager supports custom measurements and custom stimulus. If you do not want to use these features, proceed to The Analysis Process on page 81.

**Note:** Constraint Manager, when launched from Allegro Designer, does not support custom measurements or custom stimulus. The Custom Measurements tab in the Analysis Modes dialog box (Analyze – Analysis Modes) as well as the custom measurements workbook is hidden.
Without Constraint Manager, you would have to extract a net from a board layout, define any custom measurement or custom stimulus in SigXplorer, then re-apply the changes back to the net in the board layout. Because you have to do this one net at a time, this can be error prone and tedious. Because Constraint Manager has a global view of all nets in a board layout, application of custom measurements and custom stimulus is simplified.

You do not define custom measurements or custom stimulus in Constraint Manager, you only assign, manage, and analyze them. You define custom measurements and custom stimulus in SigXplorer, save them as a topology file, and import them into Constraint Manager as an ECSet (File – Import Electrical CSet). Any net-related object that references that ECSet will inherit any custom measurement or custom stimulus data that was captured in that ECSet.

In this way, an ECSet performs double-duty. Not only does an ECSet contain constraints, it can also contain custom measurements and custom stimulus.

Tip
Because you can assign only a single ECSet to a net-level object, you must define any constraint data along with custom measurement and custom stimulus in that same ECSet.

Use Model

Typically, you will select a net in Constraint Manager, click-right, then choose SigXplorer from the pop-up menu. The net’s topology will then appear in SigXplorer where you can define the necessary custom measurements and custom stimulus.

Tip
Consult SigXplorer’s online help for information about how to define custom measurements and custom stimulus.

Next, you choose File – Update to export the topology file from SigXplorer. The corresponding ECSet is refreshed in Constraint Manager and all net-related objects that reference the ECSet will inherit the custom measurements and custom stimulus that you just defined, along with any electrical constraints that were captured in the ECSet before the export to SigXplorer.
Tip

Constraint Manager retains the analysis modes settings that you define in the ECSets when you export the topology to SigXplorer. See Analyzing with Custom Measurements and Custom Stimulus on page 79 for information about analysis modes.

Managing Custom Measurements

Once defined and imported from SigXplorer, custom measurements populate an ECSets under the Custom Measurements workbook in the Net folder. Each set of custom measurements (an ECSet) appears as an individual worksheet. Each custom measurement appears as a column in the worksheet. See Custom Measurement Worksheets on page 78.

Figure 5-4 Custom Measurement Worksheets

Constraint Manager maintains custom measurement and custom stimulus associations—ECSet to object—as well as analyzed results from one session to the next.
Tip

When you select an ECSet in the Referenced Electrical CSet column of the Custom Measurements worksheet, then click-right and choose SigXplorer from the pop-up menu, that ECSet is exported from Constraint Manager to SigXplorer as a topology with custom measurements and custom stimulus intact. File – Update from SigXplorer then refreshes the custom measurements in Constraint Manager with any changes.

Analyzing with Custom Measurements and Custom Stimulus

Analyzing a net-related object with a custom measurement or a exercising with a custom stimulus involves the same steps as described in The Analysis Process on page 81. Additionally, you must follow these steps:

➤ Specify Analysis Settings

Custom measurements apply only to reflection simulations. You specify the simulation type in the Analysis Settings dialog box. If you have custom stimulus defined in the ECSet, it too must be enabled for analysis. See the Analyze Settings dialog box on page 76 for more information on how to specify the simulation type and how to enable custom stimulus.

➤ Enable Custom Measurements

Note: Constraint Manager, when launched from Allegro Designer, does not support custom measurements or custom stimulus.

You enable custom measurements through the custom measurements tab of the Analysis Modes dialog box (Analyze – Analysis Modes). Measurements appear as children in a tree structure with the parent object representing the ECSet that contains the set of custom measurements (see Analysis Modes dialog box: Custom Measurements view).
The checkbox adjacent to the parent object also serves as a toggle switch for all measurements in the ECSet: ‘all on’ (when checked) or ‘all off’ (when unchecked). Only checked measurements appear in analysis results (see Analysis Results on page 87 for more information).

➤ Analyze Custom Measurements

You do not analyze a custom measurement; rather, you analyze the object that references an ECSet which contains custom measurements.

The scope of a net object that contains a custom measurement can range from a pin-pair to a bit of a bus to an entire bus. Once you have (1) imported an ECSet that contains custom measurements, (2) assigned the ECSet to a net object, (3) specified analysis settings, and (4) enabled custom measurements, you then select the net object and choose Analyze – Analyze (or click-right and choose Analyze from the pop-up menu).

Important

As many net objects can have the same custom measurement, you must click the appropriate tab to access the object that you want to analyze. See Custom Measurement Worksheets on page 78 for a view of custom measurement worksheets and their associated tab.
Tip

You can specify analysis settings, DRC modes, custom measurements, and desired reports from a single dialog box (choose Objects–Report)

The Analysis Process

The following steps serve as a guideline (a checklist) of the steps involved in performing analysis in Constraint Manager. You may not need to perform all the steps all the time; it depends on where you use Constraint Manager in the design flow. For example, once you set DRC modes and analysis settings, you may decide to retain these settings for subsequent analysis.
**Step 1**
Create Design Objects

You want to combine objects, where appropriate, into easily-managed object groupings. In this way, constraints can be set at different levels in the object hierarchy.

- Where appropriate, combine designs into systems.

  A system configuration database is advisable for maintaining system-level constraints and design objects. See the *SPECCTRAQuest Simulation and Analysis Reference* for more information on system-level design.

- Where appropriate, combine nets and Xnets into buses

- Where appropriate, combine nets or Xnets into diff pairs.

  Each member of the diff pair must have the appropriate signal model assignment.

- Where appropriate, combine nets, Xnets, and pin-pairs into match groups.

- Where appropriate, specify pin-pair connections.

  See “Working with Objects” on page 19 for information about how to organize objects and “Working With Constraints” on page 41 for information about creating and assigning ECSets.
Step 2
Set Constraints

Next, you create ECSets based on your design requirements.

- Create an ECSet in the appropriate worksheet.

This can be done (1) from scratch in the ECSets object folder; (2), based on an existing net-related object in the Nets object folder; (3), by cloning an existing ECSet; or (4), by importing an ECSet.

Important

When specifying constraint parameters in a worksheet cell, it may be helpful to click-right and choose Change from the pop-up menu. This will guide you through the appropriate parameters and syntax that applies for the specific constraint type that the cell represents.

See “Working With Constraints” on page 41 for information about creating and assigning ECSets.
Step 3
Assign Constraints

Next, you assign ECSets to appropriate objects in your design. Child objects inherit the constraints from an ECSet assigned to a parent object.

➤ Create an ECSet in the appropriate worksheet.

This can be done (1) from scratch in the ECSets object folder; (2), based on an existing net-related object in the Nets object folder; (3), by cloning an existing ECSet; or (4), by importing an ECSet.

Important

When specifying constraint parameters in a worksheet cell, it may be helpful to click-right and choose Change from the pop-up menu. This will guide you through the appropriate parameters and syntax that applies for the specific constraint type that the cell represents.

➤ Assign the ECSet to a net-related object
-or-
Set a constraint directly on a net-related object.

If an ECSet is already assigned to that object, the constraint change that you make will override the constraint value inherited from the ECSet.

See “Working With Constraints” on page 41 for information about creating and assigning ECSets.

Step 4
Set DRC Modes

Next, you specify how Constraint Manager performs design rule checks. You may want to make a trade-off between completeness and performance.

➤ Set the appropriate mode for design rule checking as described in Analyzing for Rule-based Constraints on page 72.
<table>
<thead>
<tr>
<th><strong>Step 5</strong></th>
<th>Next, you may want to change the way Constraint Manager presents data.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Set View Options</td>
<td>➤ Ensure that the use color checkbox is enabled (<code>View – Options</code>).</td>
</tr>
<tr>
<td></td>
<td>➤ Set the desired colors to be used for results returned from analysis as described in “Cell Colors used in Analysis” on page 67</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th><strong>Step 6</strong></th>
<th>Next, you set up simulation parameters for reflection and crosstalk analysis.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Set Analysis Parameters</td>
<td>➤ Specify parameters (<code>Analyze – Settings</code>) that govern the analysis engine as described in “Analyzing for Simulation-based Constraints” on page 75.</td>
</tr>
<tr>
<td></td>
<td>For an in-depth discussion of analysis parameters, see the SPECCTRAQuest Simulation and Analysis Reference.</td>
</tr>
</tbody>
</table>
Step 7
Set Report Parameters

Next, you specify report types and what objects to include in the report. You typically will want a report when you want to analyze many objects; otherwise, it is more practical to interpret results returned to worksheet cells when you are concerned with only a handful of objects.

➤ Specify the reports that you want generated from simulation-based analysis (Objects – Report).

In the Report dialog box, you identify the ECSets, and net-related worksheets, to be included in the analysis results.

You can limit the report to specific object types (bus, diff pair, Xnet, net, ECset), and to a specific condition (any condition, only violations, only failures, only objects that are constrained).

Note: Incidentally, from the Report dialog box, you can also specify DRC modes and analysis settings, and you can initiate simulation-based analysis.

For an in-depth discussion of reports, measurements, and computations, see the SPECCTRAQuest Simulation and Analysis Reference.

Step 8
Select an object

Next, you choose which objects to analyze. Worst-case results of child objects roll up to the respective parent object.

➤ Specify a net, Xnet, or object grouping to be analyzed.

➤ Once in view, click in a cell in the object column.

You can select a range of cells using SHIFT-Click and non-contiguous cells by using CNTRL-click.
Step 9
Analyse

Finally, you initiate the simulation(s).

➤ Choose Analyse – Analyse (or click-right and choose Analyse from the pop-up menu).

**Important**
As the analysis progresses, you can receive feedback by monitoring the status bar (located at the lower-left corner of Constraint Manager).

Analysis Results

Results returned from Analysis take four forms:

- Generated DRCs in the layout
- Waveforms
- Reports
- Calculated *actuals* and *margins* populated in the worksheets

Each is discussed in the sections that follow.

**Generated DRC Output**

Updated constraint information is communicated to Allegro/APD or SPECCTRAQuest. If a violation exists, a DRC bow tie marker is attached to the offending object in the layout.

**Waveforms**

Analysis results returned for certain constraints in the *signal integrity* and *timing* worksheets yield waveform files. In Constraint Manager, choose *Tools – SigWave* to view these waveforms.

Analysis results returned for SSN constraints in the *signal integrity* worksheet yield waveform files for viewing plane noise. In Constraint Manager, choose *Tools – EMWave* to view these waveforms.
Reports

For each enabled net-related worksheet or ECSet, a report is produced, consmgr.rpt, that lists constraint parameters, object assignments, and analysis results.

Worksheet cells

Analysis results returned to worksheet cells exhibit the following behavior.

- Cells give graphical feedback to reflect their status. See Cell Colors used in Analysis on page 67 for more information on default and user-defined colors. By default, the following color scheme is used for analysis:
  - Pass = green
  - Fail = red
  - Analysis error = yellow
  - Directly set = blue

- Cells that are grayed-out reflect that the cell is not applicable for the selected object.

- Cells will be colored blue if the cell contains a value which has been explicitly entered. This could happen when you override, for example, one bit of a bus object or when you specify a constraint directly on a net-related object rather than having that object inherit its constraint value from a referenced ECSet.

- Cells which are populated and colored black reflect that the value is inherited from a higher-level cell or an ECSet reference on the object. When you select an inherited cell, the status bar will indicate the source of the value. The source (the owner of the object) is reported as the object type and its name.
Interpreting Analysis Results Returned to a Worksheet

Figure 5-6 and Table 5-4 take you through a typical scenario of analyzing for propagation delay. Together, they explain how to interpret the analyzed results fed back to the worksheet.

Figure 5-6  Analyzing for Propagation Delay

Table 5-4  Dissecting the Analyzing for Propagation Delay figure on page 89

<table>
<thead>
<tr>
<th>Object</th>
<th>Cell Column</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>LMD_BUS</td>
<td>Referenced</td>
<td>ECSets are set directly on the bus-level object. The cell is rendered blue.</td>
</tr>
<tr>
<td></td>
<td>Electrical CSet</td>
<td>Members of the bus will inherit the constraint values set on the bus. This is evident in the individual nets under the expanded MAB_BUS. Inherited constraint values are rendered black.</td>
</tr>
</tbody>
</table>
### Table 5-4 Dissecting the Analyzing for Propagation Delay figure on page 89

<table>
<thead>
<tr>
<th>Object</th>
<th>Cell Column</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>LMD_BUS</td>
<td>Min Delay (Actual/Margins)</td>
<td>Cells are rendered green and do not contain values. This indicates that the last time the object (LMD_BUS) was analyzed, it was within the specified constraint values. For example, if the board was analyzed in an earlier design session, the analyzed values would not be saved with the board database. However, the last analyzed state of the object (pass, in this case) is communicated back to the cell in the form of a solid color. To populate the cells with integral values, you must re-run analysis (Analyze – Analyze). You could also import saved analysis results (File – Import – Analysis results).</td>
</tr>
<tr>
<td></td>
<td>Max Delay (Actual/Margins)</td>
<td></td>
</tr>
<tr>
<td>MAB_5</td>
<td>Min Delay (Min)</td>
<td>Nets 5 and 8 of MAB_BUS have overrides. Because the overrides were specified explicitly in each cell, the cell is rendered blue. Notice that all other members of MAB_BUS inherit their values from the constraint specified at the bus level. Therefore, these cells are rendered black.</td>
</tr>
<tr>
<td>MAB_8</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MCKE_BUS</td>
<td>Min Delay/Max Delay</td>
<td>Analysis failed, rendering the cells yellow. This was caused by an unplaced component attached to a net member of this bus.</td>
</tr>
<tr>
<td>MAB_4</td>
<td>Min Delay (Actual/Margin)</td>
<td>Analysis passes, rendering the cells green. Notice that only the margin column contains an integral value; the actual is solid. This is because the net has several hidden pin-pairs. Since the cell can contain only one value, the cell is rendered a solid color to represent a pass/fail condition.</td>
</tr>
<tr>
<td></td>
<td>Max Delay (Actual/Margin)</td>
<td></td>
</tr>
<tr>
<td>MAB_1</td>
<td>Min Delay (Actual/Margin)</td>
<td>Analysis passes, rendering the cells green. Notice that both the margin and the actual columns contain integral values. This is because the net has been completely expanded (bus, to net, to pin-pair).</td>
</tr>
<tr>
<td></td>
<td>Max Delay (Actual/Margin)</td>
<td></td>
</tr>
</tbody>
</table>
Table 5-4 Dissecting the Analyzing for Propagation Delay figure on page 89

<table>
<thead>
<tr>
<th>Object</th>
<th>Cell Column</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>MAB_BUS</td>
<td>Min Delay</td>
<td>Analysis is in violation, rendering the cells red.</td>
</tr>
<tr>
<td>MAB_13</td>
<td>(Actual/Margin)</td>
<td>Notice that both the margin and the actual columns contain integral values at the pin-pair level of the MAB_13 net. This is because the net has been completely expanded (bus, to net, to pin-pair). Also, notice that the net object that owns the pin-pair displays a solid red in the actual column and an integral value in the margin column. This is because the worst-case violation is rolled up to the object that owns it. In this example, there is only one pin-pair so it was rolled up. Again, if there were more than one pin-pair in violation, since the actual cell can contain only one value, the cell would be rendered a solid color to represent a pass/fail condition.</td>
</tr>
</tbody>
</table>

Important

Constraint violations on child objects are rolled up the object hierarchy to the parent object. That is, pin-pairs roll up to the parent net or Xnet, nets or Xnets roll up to the parent bus, and buses roll up to the parent design. In this way, you can work at any level in the object hierarchy and still be informed of a constraint violation on a lower-level object that is hidden.

Finally, the same worst-case pin-pair violation on the MAB_13 net is rolled up to the parent bus, MAB_BUS.
Constraints Across the System

A system configuration represents the electrical characterization of a system including all the participating designs, including interconnecting cables and connectors, as well as Xnets and pin-pairs and their assigned ECSets.

**Note:** Constraint Manager, when launched from Allegro Designer, does not support board-to-board constraints.

You can set a constraint directly on a system-Xnet in your layout or you can define the constraint in Constraint Manager as an ECSet and then reference it to a system-Xnet.

If any design-Xnet is part of a bus or a diff pair object, the system-Xnet will also be part of that bus or diff pair. You do not have to define same bus object in all designs.

See the *SPECCTRAQuest Simulation and Analysis Reference* for a thorough discussion of system-level designs.
Using Constraint Manager in the High Speed Design Flow

Topics in this chapter include

- Phases in the Design Flow on page 94
- Design Exploration Phase (with SigXplorer) on page 95
- Design Capture Phase (with Concept HDL) on page 97
- Design Floorplanning and Implementation Phases (with SPECCTRAQuest and Allegro) on page 106
Phases in the Design Flow

A typical high-speed design flow contains the following phases.

- Exploration
- Capture
- Floorplanning
- Implementation

Each phase in the design flow requires different tools. Constraint Manager provides a common environment for managing high-speed electrical constraints across all tools in the design flow.

**Note:** Constraint Manager, launched from Allegro Designer, does not support topology exploration with SigXplorer and design capture and database synchronization with Concept HDL.

Not all phases in the design flow are mandatory. For example, a new design may be a derivative of a prior design. In this case, the exploration and floorplanning phases may not be needed.

**Figure 6-1  Tools in the Design Flow**

Constraint information in the board and in the schematic databases are synchronized using Design Sync. With Design Sync, you can specify that all constraints be synchronized or only those which have changed.
The sections that follow describe how to use Constraint Manager with other tools at each phase in the design flow.

**Design Exploration Phase (with SigXplorer)**

In the exploration phase, you focus on up-front exploration before the board is placed and routed. Board cross-section and material type are usually *not* known, although you can make assumptions from past designs. A netlist is *not* available in this phase of the design flow.

SigXplorer can be used to perform simulations based upon the ECSets characteristics (pins, scheduling, models). A unique topology template can be saved for each point explored in the solution space. The end result of the exploration phase is to create a library of ECSets (.top files on disk) which would then be imported back in to Constraint Manager where they could be swapped in and out with other ECSets or where individual constraints could be moved between ECSets.

In the exploration phase, you have a choice. Constraints can be proven in SigXplorer and saved as topology templates or they can be defined in Constraint Manager. The primary difference is presentation: SigXplorer is form-based; Constraint Manager is worksheet-based and perhaps it is easier to use for viewing and manipulating multiple constraint definitions.

**Note:** You'll notice that only the **ECSets** folder is shown in Constraint Manager's worksheet selector. Absent of a board database, and a netlist, Constraint Manager does not show the **Nets** folder. See the Workbooks and Worksheets figure on page 13 for information about the Nets folder.

Also, without a database with which to save constraint data, before exiting SigXplorer, or Constraint Manager, you must ensure that you save to a topology template to preserve your work.

**Tip**

You also use SigXplorer in the Constraint Manager flow to define custom measurements and custom stimulus. See **Custom Measurements and Custom Stimulus** on page 76 for more information.
In SigXplorer, you simulate and analyze the topology. The following can be captured in a topology template:

- pin ordering (topology scheduling)
- termination strategy (and location on net)
- electrical constraints
- custom measurements
- custom stimulus

Once exploration has been completed, you save this information as a topology template (.top file). This file represents the SigXplorer database. Constraint Manager is later used to import this information as an ECSet.

**Pin Scheduling**

In Constraint Manager, you can select from the following pre-defined pin scheduling topologies:

- minimum spanning tree
- star
- daisy chain
- source load daisy chain
- far-end cluster

These choices can be made from the wiring worksheet of the routing workbook. If you want to define your own pin schedules, you must manually wire the connections in SigXplorer and then export this information (File – Update) back to Constraint Manager.
Design Capture Phase (with Concept HDL)

In the design capture phase, you focus on capturing constraints as you implement logic. You use Constraint Manager along with Concept HDL to manage electrical constraints.

**Note:** Constraint Manager, when launched from Allegro Designer, does not support design capture and database synchronization with Concept HDL.

---

**Important**

This section focuses on using Concept HDL in the ‘CM-enabled’ design flow. To use this flow, you must be using the 14.2 versions of Concept HDL and Constraint Manager. To support the ‘CM-enabled’ design flow, Packager XL uses additional feedback files (*pst*.dat) as does genfeedformat (*view.dat). See Figure 6-3 on page 103 and Figure 6-4 on page 105 for more information on front-to-back and back-to-front flows, respectively. Once you move from the ‘traditional’ design flow to the ‘CM-enabled’ design flow, you cannot revert back.

---

**Tip**

The Working with Electrical Constraints chapter of the *Concept HDL User Guide* contains detailed information about using Concept HDL in both the traditional- and the CM-enabled-flow.
Constraint creation or modifications in Constraint Manager are immediately synchronized with the schematic's occurrence property files when you save (in Constraint Manager, choose File – Save). Any electrical constraints which are defined directly in the schematic must be explicitly updated (in Concept HDL, choose Tools – Constraint Manager – Update Schematic).

You can also use SigXplorer in this phase to perform simulations based upon the ECSet's characteristics (pins, scheduling, models, custom measurements and custom stimulus) of the net-related objects in your design.

- You launch SigXplorer from Constraint Manager by selecting a net-related object, or an ECSet, and choosing Tools – SigXplorer. You can also click-right and choose SigXplorer from the pop-up menu.

See Using SigXplorer in the capture, floorplanning and implementation phases on page 109 for information on using SigXplorer.

**Using Constraint Manager with Concept HDL**

You can concurrently create and modify electrical constraints in Concept HDL and in Constraint Manager; design sync mechanisms promote the same constraint definitions and modifications regardless of where you make the changes.
Tip

We suggest that you use Constraint Manager as the primary, and perhaps the only, method of defining electrical constraints. You may, however, have the occasional need to define an electrical constraint directly in Concept HDL.

Constraint edits made within Constraint Manager are synchronized to Concept HDL’s schematic view. Conversely, constraint edits made in Concept HDL are synchronized to the Constraint Manager Database (CMDB).

The CMDB is, in effect, a view of the Concept HDL database called the constraints view, and it is saved in the dictionary and constraints file `designname.dcf`.

Invoking Constraint Manager from Concept HDL

When launching Constraint Manager from Concept HDL with schematic changes pending, a prompt will remind you to save the changes to the schematic before Constraint Manager can be launched. This is to ensure that Constraint Manager accurately reflects the latest connectivity and electrical constraint data. Additionally, you must be working in expanded mode.

➤ To launch Constraint Manager from Concept HDL, choose Tools – Constraints – Edit.

Important

You cannot edit electrical constraints in Concept HDL (text attributes attached to a net) when Constraint Manager is running.

Working in Constraint Manager

When you edit a constraint in Constraint Manager and then save in either Constraint Manager or in Concept HDL (File – Save), the change is immediately propagated to the occurrence property file (OPF) of the schematic and is immediately reflected in the attribute dialog box in Concept HDL.
If you also want to see the constraint edits made in Constraint Manager reflected in the schematic, choose Tools – Constraints – Update Schematic (or File – Export Physical followed by Tools – Backannotate) from Concept HDL. Use the latter if you want to also update the schematic with package and connectivity information.

Tip

In Constraint Manager, you can perform an audit (Audit – Obsolete Objects) to ensure that objects in the Constraint Manager database also exist in the schematic. See Obsolete Objects Audit on page 60 for more information on the audit functions.

Additionally, you should ensure that net names are the same before you constrain them in either Concept HDL or in Constraint Manager. After a net is constrained, you should not rename it. Again, the Audit commands can be used to resolve net naming conflicts between both databases.

Constraint Manager running with Concept HDL cannot intelligently map the constraint information imported from a topology template, or defined in an ECSet, to a candidate net that matches the topological characteristics of the referenced ECSet. Therefore, all topology-related constraints, scheduling, and specific pin-pairs cannot be applied until the design is opened in Allegro, SPECCTRAQuest, or APD. See “Mapping Templates and ECSets to Net-related Objects” on page 56 for information on the applying ECSet constraints.

Tip

Until the design is packaged, net names in Constraint Manager appear in canonical (logical) form. After packaging, you can use Constraint Manager to edit constraints on nets using physical (packaged) net names.

Working in Concept HDL

When working in Concept HDL without Constraint Manager running, you can use Concept HDL's attribute editor to define or edit constraints. When you invoke Constraint Manager from Concept HDL and save the schematic, all properties that you edited in Concept HDL will appear in the appropriate worksheets in Constraint Manager. See Invoking Constraint Manager from Concept HDL on page 99.

When working in Concept HDL with Constraint Manager running, you cannot edit constraints in Concept HDL directly. You can, however, set an attribute placeholder so that constraint modifications in Constraint Manager can refresh the schematic after a back-annotation (choose Tools – Backannotate from Concept HDL).
To set an attribute placeholder, in Concept HDL choose *Text – Attributes*, specify a constraint name with a ‘?’ value and choose *Value* from the Visible drop-down menu.

**Important**

You cannot use a placeholder at the pin-pair level.

In addition to assigning individual properties to a net in Concept HDL, you can reference an ECSet in Constraint Manager. In this way, many properties can be managed as a unit.

To reference an ECSet, add the `ELECTRICAL_CONSTRAINT_SET` property to a net in Concept HDL and furnish the name of the ECSet, as it appears in Constraint Manager, as its value.
You should consider the following when using Concept HDL with Constraint Manager.

**Important**

- To pass high-speed electrical properties between the front- and the back-end tools, you must:
  - Enable net properties for annotation
    
    In the Packager Setup dialog box, click the From Layout tab, then enable (check) the Net option in the Annotate field.
  - Ensure that the properties are enabled in the transfer list
    
    In the Packager Setup dialog box, click Property Flow Setup, then enable the desired properties in the Transfer column.
  - Ensure that the property has a placeholder in the schematic
    
    See Figure 6-2 on page 101.
  - Enable back-annotation
    
    Choose Tools – Backannotate in Concept HDL or enable Backannotate Schematic in the Export- or Import Physical dialog boxes.
- A net-level property in Concept HDL overrides a constraint value inherited from an ECSet in Constraint Manager
- You must have the correct package information to define a pin-pair constraint in Concept HDL or in Constraint Manager
- If you change the package information, some pin-pair data may become obsolete
- Constraint Manager does not read the constraints view of lower-level blocks in a hierarchical schematic
- You must be in occurrence edit mode to refresh a value at the bus level
- A constraint that you delete in Concept HDL will not be reflected in Constraint Manager. Instead, you should delete the constraint in Constraint Manager and choose File – Save. The corresponding constraint will then be deleted in Concept HDL as well.
Front-to-Back Constraint Flow

In the front-to-back constraint flow (see Figure 6-3 on page 103), electrical constraint and netlist information is exported from Concept HDL (File – Export Physical) and imported into SPECCTRAQuest or Allegro/APD (File – Import Logic).

Tip

Alternatively, you can use Project Manager to streamline the flow of information among tools: (1) Click the Design Sync icon; (2), click Export Physical from the pop-up menu; (3), ensure that the Package Design and Update Allegro Board (Netrev) options are checked; and (4), click OK.

Important

The Constraint Manager-enabled high-speed design flow requires that 5 PST files be passed from the front-end to the back-end.
In the front end, electrical constraint export is controlled by Concept HDL's Export Physical dialog box. Furthermore, the *Update Electrical Constraints* checkbox is forced-enabled (you cannot change this setting), and you can choose one of the following mutually exclusive radio buttons:

- **Overwrite**—all existing electrical constraint information in the *Output Board File* will be overwritten with the electrical constraint information currently available in the project.

- **Changes only**—only the electrical constraint information which has changed since the last export will be written to the *Output Board File*.

⚠️ **Important**

You can control the flow of constraints, front-to-back, entirely from the front-end by enabling the ‘*Update Allegro Board (Netrev)*’ option as specified in Concept HDL's File Export dialog box.

In the back end, electrical constraint import is controlled by Allegro's Import Logic dialog box. For the CM-enabled front-to-back flow, you can choose from one of the following mutually exclusive radio buttons:

- **Overwrite current constraints**—all existing electrical constraint information will be overwritten.

- **Import changes only**—only the electrical constraint information that has changed since the last import will be imported.

💡 **Tip**

The Working with Electrical Constraints chapter of the *Concept HDL User Guide* contains detailed information about using Concept HDL in both the traditional- and the CM-enabled-flow.

**Back-to-Front Constraint Flow**

In the back-to-front constraint flow (see Figure 6-4 on page 105), electrical constraint and netlist information is exported from SPECCTRAQuest or Allegro/APD (*File – Export Logic*) and imported into Concept HDL (*File – Import Physical*)
Tip

Alternatively, you can use Project Manager to streamline the flow of information among tools: (1) Click the Design Sync icon; (2), click Import Physical from the pop-up menu; (3), ensure that the Generate Feedback Files and Package Design options are checked; and (4), click OK.

Figure 6-4  CM-enabled back-to-front flow

In the front end, the electrical constraint import is controlled by Concept HDL’s Import Logic dialog box. The Feedback Source field must specify Allegro (radio button depressed). For the CM-enabled back-to-front flow, you can choose from one of the following mutually exclusive radio buttons.
Constraint Manager Design Guide
Using Constraint Manager in the High Speed Design Flow

- **Overwrite current constraints**—the current electrical constraint information in the project will be overwritten with the electrical constraint information from the Allegro board.

- **Import changes only**—only the electrical constraint information that has changed since the last import will be updated in project.

**Note:** Alternatively, it is possible to control the flow of constraints, back-to-front, entirely from the front-end, as specified in Concept HDL’s File Import dialog box.

**Tip**

The Working with Electrical Constraints chapter of the *Concept HDL User Guide* contains detailed information about using Concept HDL in both the traditional- and the CM-enabled-flow.

### Design Floorplanning and Implementation Phases (with SPECCTRAQuest and Allegro)

In the floorplanning and implementation phases, you focus on placement, routing, and manufacturing output. This section focuses on using Constraint Manager with back-end tools. For information on the front-to-back flow, you should also refer to Design Capture Phase (with Concept HDL) on page 97.

**Note:** Constraint Manager, when launched from Allegro Designer, does not support topology exploration with SigXplorer.

Constraint Manager is used along with SPECCTRAQuest or Allegro/APD to manage electrical constraints. Constraint creation or modifications in Constraint Manager will automatically be synchronized with the board (.brd) database.
SigXplorer can also be used to perform simulations based upon the ECSets' characteristics (pins, scheduling, models) of the net-related objects in your design. See *Using SigXplorer in the capture, floorplanning and implementation phases* on page 109 for information on using SigXplorer.

- You launch Constraint Manager from SPECCTRAQuest or from Allegro/APD (*Setup – Electrical Constraint Spreadsheet*).
- You launch SigXplorer from Constraint Manager by selecting a net-related object (or an ECSet) and choosing *Tools – SigXplorer*. You can also click-right and choose *SigXplorer* from the pop-up menu.

In the floorplanning and implementation phases, you use Constraint Manager to:

- Migrate constraint sets, from older, pre-14.0, databases into ECSets used in Constraint Manager.
  See *Topology Templates Audit* on page 61 as well as *Appendix A.* for instructions.
- Import reusable topology templates from SigXplorer. These map to ECSets in Constraint Manager.
  See *Importing ECSets* on page 54 for information on using reusing topology template files from SigXplorer.
- Consolidate individual Nets and Xnets into more easily-managed units such as buses and match groups.
  See *Working with Objects* on page 19 for information on buses and match groups.
- Define bus, diff pair, net, Xnet, or pin-pair constraints.
  See *Working with Objects* on page 19 for information on objects in Constraint Manager.
- Define diff pairs based on signal model assignment.
  See *Diff Pair* on page 23 and the *SPECCTRAQuest Simulation and Analysis Reference* for information on diff pairs and signal models.
- Define net-related constraint overrides, as appropriate.
  See *Electrical Constraint Sets* on page 42 for information on overriding a constraint.
- Manage total etch length constraints on each net / Xnet in the design.
  See “*Total Etch Length*” on page 32.
- Create ECSets based on net-related objects such as buses, diff pairs, nets, and Xnets.
  See *Operations on ECSets* on page 47 for information on creating ECSets.
Constraint Manager Design Guide
Using Constraint Manager in the High Speed Design Flow

- Explore net topologies and schedule pins.
  See Pin Scheduling on page 96 for information on pre-defined pin schedules.

- Audit ECSets to resolve inconsistencies.
  See Auditing ECSets on page 59 for information on constraints and their assignments.

- Validate the design through design rule checks and analysis.
  See Chapter 5, “Constraint Analysis” for more information on validating constraints.

- Communicate layout changes to Concept HDL.
  See Design Capture Phase (with Concept HDL) on page 97 for more information on the front-to-back constraint flow.
Using SigXplorer in the capture, floorplanning and implementation phases

**Note:** Constraint Manager, when launched from Allegro Designer, does not support topology exploration with SigXplorer and design capture and database synchronization with Concept HDL.

Unlike in the exploration phase, where there is no board or netlist available, SigXplorer employs a different use model in the floorplanning and implementation phases.

SigXplorer can be used to extract a net (or a net-related object such as a bus, diff pair, or match group) for topology exploration and constraint modification. The extraction can be routed (a trace in SPECCTRAQuest, Allegro, or APD) or unrouted (a ratsnest). Used in this way, SigXplorer is aware of the electrical and physical characteristics of the net.

You also use SigXplorer in the Constraint Manager flow to define custom measurements and custom stimulus. See [Custom Measurements and Custom Stimulus](#) on page 76 for more information.

- To extract a net-related object, select a net in worksheet, then click-right and choose *SigXplorer* from the pop-up menu

**SigXplorer will:**

- Extract all electrical constraint and topology information from the selected object.
  - If the *Use Include Routed Interconnect* box is checked (*Tools – Options* in Constraint Manager), interconnect details (clines and vias) will be included.
  - If the *Use Actuals* box is checked (*Tools – Options* in Constraint Manager), the actual routed delays will be included.
  - If the selected object is a Bus or Diff Pair, the template will include information from the *first* Xnet or Net.

- Display the appropriate ratsnest based upon the chosen topology schedule:
  - for pre-defined scheduling, this choice is the value of the `RATSNEST_SCHEDULE` property. See [Pin Scheduling](#) on page 96 for information on pre-defined pin schedules.
  - for user-defined scheduling, this choice is the value of the `TEMPLATE` property. See the online help for instructions on scheduling topologies.
You then simulate and analyze the topology, and make trade-off decisions.

The ECSet will be refreshed in Constraint Manager after choosing *File – Update* in SigXplorer.
Migrating Pre 14.0 Electrical Constraints
Overview

Designs created using release 13.6 (prior to the release of Constraint Manager) contain electrical constraints that you carry forward into Constraint Manager as part of the process of up-reving (converting) your design databases for compatibility with the current release.

To understand this process, let’s review how electrical constraints were managed in release 13.6.

Managing Constraints in Release 13.6

Electrical Rule Sets

In release 13.6, you defined electrical rules using the Electrical Rule Set dialog box shown in Figure Figure A-1 on page 113.

➤ To access the Electrical Rule Set dialog box, from SPECCTRAQuest choose Constraints – Edit Constraint Sets and then click the Create Constraints button.
In this example, there are four Electrical Rule Sets. Three (Address, Analog and Data) were created. The fourth (Default) is supplied for every design and applies to all nets not specifically assigned to any other constraint set.

Topology Templates

In release 13.6, topology templates were applied to a database either through the netlist with the ASSIGN_TOPOLOGY property or directly through the topology template dialog box. Once applied to target nets, all of the properties from the topology template became net level properties in the database. The references to the original topology template were maintained with the TOPOLOGY TEMPLATE property on nets.

Net Properties

Other constraints were set directly on the net either from the schematic or directly in Allegro, SPECCTRAQuest, or APD. These net level properties would take precedence over any constraints inherited from an Electrical Rule Set.
Next, let's examine what happens after you uprev a design to release 14.0.

Managing Constraints with Constraint Manager

Electrical Rule Sets

After invoking Constraint Manager on an up-reved design for the first time, open any Electrical Constraint Set worksheet such as *All Constraints*. The *Objects* column for any of these worksheets lists all of the Electrical Constraint Sets (ECSets) that exist in the design.

Figure A-2 Electrical Rule Sets as ECSets in Constraint Manager

In this example, there are three electrical constraint sets listed (ADDRESS, ANALOG, DATA); they were Electrical Rule Sets in 13.6 (see Figure A-1 on page 113). Selecting any of these ECSets and choosing *Objects* – *Electrical CSet References* reveals the list of nets (if any) that are assigned to that ECSet.

At this point the constraint values associated with each ECSet should be checked to determine if the ECSet is still valid and whether it should be retained. Also, an ECSet cannot be deleted until you remove all references to it.
The UPREVED_DEFAULT ESet

**Note:** For many up-reved designs, DEFAULT will be the only ESet that appears in the list.

The DEFAULT Electrical Rule Set from a 13.6 design is handled as follows:

- If the DEFAULT rule set contained any values in the 13.6 design, it is migrated to 14.0 as the UPREVED_DEFAULT electrical constraint set.
- The UPREVED_DEFAULT electrical constraint set is referenced to every net in the design that did not reference any other rule set in 13.6.

**Tip**

Most of the time this will be every net in the design. Check the values for constraints in this constraint set. It is likely that there was some constraint value which was set to zero and the DRC for that constraint was never checked in 13.6.

Unless there is a constraint that you want to manage in this manner, all references to this constraint set should be removed (choose Objects – Electrical CSet References). You should then delete the constraint set.

**Topology Templates**

If any Net worksheets were opened (prior to any of the steps above), you may have observed the following:

- Existing values in the Referenced Electrical CSet column. These came from 13.6 Electrical Rule Sets.
  
  **Note:** If a Referenced ESet is set on every net, it is most likely to be the UPREVED_DEFAULT constraint set.

- Constraint values set directly on nets. These appear in a dark blue font indicating that they are set directly on the net as properties. These values in blue came from net level properties in 13.6.
  
  **Note:** At this point, it’s unclear if these properties were set directly or if they came from a topology template.

In 14.0, net properties are not used since all electrical constraints are defined in an Electrical Constraint Set (ESet). A topology template in 14.0 is an ESet by definition. For details, see Chapter 4, “What is a Topology Template?”.
To properly update an existing 13.6 board with net constraints from a topology template to a 14.0 board with ECSets, you must perform the following.

1. Audit the templates. In Constraint Manager, choose Audit – Topology Templates. If the following confirmer appears, then there are no existing properties on nets (ASSIGN_TOPOLOGY, TOPOLOGY_TEMPLATE) indicating that a Topology Template was assigned or is impending an assignment.

**Figure A-3 Audit Topology Template Confirmer**

![Audit Topology Template Confirmer](image)

If there are nets that need updating, the following dialog box appears.

**Figure A-4 Audit Topology Properties Dialog Box**

![Audit Topology Properties Dialog Box](image)

The top left combo box has one entry for each topology template property in the design. The list box below it contains all of the nets that reference the selected topology template.

2. Choose which template to update and then use the Update to reference Electrical Cset section of the dialog box to select the appropriate reference. Most likely, this will be the Import option so you can search for the original topology template on disk with the Browse... button.

**Note:** If the topology templates are in the same directory, the path may already be seeded with the correct file.
3. Select *Override existing constraints*. This option will delete the old net constraints so that all of the constraints will be inherited from the updated ECSet reference.

**Tip**

Make sure that the topology templates are as intended because this button will also override existing constraints if the ECSet has different constraints than the 13.6 net properties.

4. Click *Apply* and you should see Constraint Manager update with the new constraints. The *Referenced Electrical CSet* column in any of the *Net* worksheets should now contain the new ECSet name. There should also be a *topology.log* file popping up with an explanation of what was processed.

**Note:** If the *topology.log* file did not pop up, then you need to verify that the *Tools – Options…Automatic topology update* option is selected, otherwise the *mapping* will not occur.

*Mapping refers to the process of matching ECSets to target nets to ensure that the constraints in the ECSet will properly apply to the referenced nets. For details, see Chapter 4, “Mapping Templates and ECSets to Net-related Objects”*

At this point, the Audit Topology Properties dialog box is ready for the next template. Repeat the same process for each template.

**Designs with many topology templates**

Perform the following if you need to update many topology templates.

1. In Constraint Manager, *deselect Tools – Options…Automatic topology update*.

   Deselecting this option is helpful for large designs with many templates and thousands of nets; each with many pin pair constraints. It could take awhile for the mapping to update. The update procedure is slightly different in this situation.

2. To import the topology templates into Constraint Manager and create the ECSets, choose *File – Import – Electrical CSets*. You can select as many topology files as you want in the file browser using the Ctrl or Shift keys.

3. Examine each ECSet in Constraint Manger and make appropriate edits to each, either directly in the worksheets or by editing each one in *SigXplorer* (right mouse button option when an ECSet is selected). For example, you may want to make sure each ECSet has the desired Topology Wiring Schedule mode.

4. Choose *Audit – Topology Templates*.
5. Choose which template to update and then use the *Update to reference Electrical Cset* section of the dialog box to select the appropriate reference. The choice will come from the combo box next to the *Existing* radio button.

6. Click *Apply* and move on to the next topology property.

7. After auditing all the templates, select the *Tools – Options… Automatic topology update* option. Be sure the *Tools – Options… Overwrite existing constraints* option is also selected if desired.


All ECsets are now mapped and assigned.

**Net Properties**

Nothing special needs to be done with net level properties in release 14.0. If they were the result of a topology template, then they will be removed as part of the previous procedure. With Constraint Manager, the goal is to manage constraints *hierarchically*. This aids in the editing and updating process because an entire bus can be updated, for example, by editing a single value on an ECSet. Net level properties still take precedence over any constraints inherited from an ECSet so they can be used as specific overrides as desired. If a particular net is not part of an ECSet, constraints can still be managed at the net level if so desired.

Sometimes, the original topology template is not available during the update process (*Audit – Topology Templates*). If so, make note of the nets that reference the missing topology template. If the topology template had already been applied to the design in 13.6, then each of the nets will have all of the properties that were originally contained in the topology template. Open any *Net* worksheet and select one of the desired nets in the *Objects* column.
1. Choose *Objects – Create – Electrical CSet.*

   The following dialog box appears.

**Figure A-5 Create Electrical CSet Dialog Box**

2. Enter a name for the new Electrical CSet and make sure *Copy Constraints From* option is selected. Otherwise, an empty ECSet will be created.

   You now have an existing ECSet in the design to use with the *Audit – Topology Templates...* command. You can also create the ECSet by editing the net in *SigXplorer* and then choosing *File – Update.* This process will create the ECSet in Constraint Manager as well.
Property Mapping

Topics in this appendix include

- **Overview** on page 122
- **Workbooks under the ECSets folder** on page 122
- **Workbooks under the Net folder** on page 126
Overview

Constraint Manager organizes constraints by workbook, then by worksheet, then by cell. Workbooks can be generic, such as those under the ECSet folder, or they can be net-related. See “Workbooks” on page 12 for information on workbook hierarchy.

This appendix depicts the cell name, as shown in Constraint Manager, with the associated property that is stored in the Concept HDL schematic or in the Allegro database. Consult the PCB Systems Properties Reference for property definitions.

➤ Tables B1, B2, and B3 present constraints contained in the ECSet folder
➤ Tables B4, B5, and B6 present constraints contained in the Net folder

You cannot edit cells that contain Actual or Margin calculations; therefore, these cells are not presented in the worksheets under the Net folder.

The All Constraints workbook in the ECSet folder presents a flattened view of all constraints under the ECset folder. Because they are described elsewhere, cells in the All Constraints folder are not presented in these tables.

Workbooks under the ECSet folder

Properties in the signal integrity workbook

Note: Constraint Manager, when launched from Allegro Designer, does not support the signal integrity workbook.

Table B-1 Signal Integrity Workbook

<table>
<thead>
<tr>
<th>Worksheet</th>
<th>Column Heading</th>
<th>Cell Label</th>
<th>Property Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reflection/Edge Distortion</td>
<td>Reflection</td>
<td>Overshoot</td>
<td>MAX_OVERSHOOT</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Min Noise Margin</td>
<td>MIN_NOISE_MARGIN</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Edge Sensitivity</td>
<td>EDGE_SENS</td>
</tr>
<tr>
<td></td>
<td></td>
<td>First Incident</td>
<td>FIRST_INCIDENT</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Switch</td>
<td></td>
</tr>
</tbody>
</table>
### Table B-1 Signal Integrity Workbook

<table>
<thead>
<tr>
<th>Worksheet</th>
<th>Column Heading</th>
<th>Cell Label</th>
<th>Property Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>Xtalk/SSN</td>
<td>Xtalk</td>
<td>Active Xtalk Window</td>
<td>XTALK_ACTIVE_TIME</td>
</tr>
<tr>
<td>Xtalk/SSN</td>
<td>Sensitive Xtalk Window</td>
<td></td>
<td>XTALK_SENSITIVE_TIME</td>
</tr>
<tr>
<td></td>
<td>Max Xtalk</td>
<td></td>
<td>MAX_XTALK</td>
</tr>
<tr>
<td></td>
<td>Max Peak Xtalk</td>
<td></td>
<td>MAX_PEAK_XTALK</td>
</tr>
<tr>
<td>Max SSN</td>
<td>Not Applicable</td>
<td></td>
<td>MAX_SSN</td>
</tr>
</tbody>
</table>

### Properties in the Timing workbook

**Note:** Constraint Manager, when launched from Allegro Designer, does not support the timing workbook.

### Table B-2 Timing Workbook

<table>
<thead>
<tr>
<th>Worksheet</th>
<th>Column Heading</th>
<th>Cell Label</th>
<th>Property Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>Switch/Settle Delays</td>
<td>Min First Switch</td>
<td>Not Applicable</td>
<td>MIN_FIRST_SWITCH</td>
</tr>
<tr>
<td></td>
<td>Max Final Settle</td>
<td>Not Applicable</td>
<td>MAX_FINAL_SETTLE</td>
</tr>
</tbody>
</table>
## Properties in the Routing workbook

<table>
<thead>
<tr>
<th>Worksheet</th>
<th>Column Heading</th>
<th>Cell Label</th>
<th>Property Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wiring</td>
<td>Topology</td>
<td>Mapping Mode</td>
<td>TOPOLOGY_TEMPLATE_MAPPING_MODE</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Verify Schedule</td>
<td>NET_SCHEDULE</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Schedule</td>
<td>RATSNEST_SCHEDULE</td>
</tr>
<tr>
<td></td>
<td>Stub Length</td>
<td>Not Applicable</td>
<td>STUB_LENGTH</td>
</tr>
<tr>
<td></td>
<td>Max Via Count</td>
<td>Not Applicable</td>
<td>MAX_VIA_COUNT</td>
</tr>
<tr>
<td></td>
<td>Max Exposed Length</td>
<td>Not Applicable</td>
<td>MAX_EXPOSED_LENGTH</td>
</tr>
<tr>
<td></td>
<td>Max Parallel</td>
<td>Not Applicable</td>
<td>MAX_PARALLEL</td>
</tr>
<tr>
<td>Impedance</td>
<td>Impedance</td>
<td>Target</td>
<td>IMPEDANCE_RULE</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Tolerance</td>
<td>IMPEDANCE_RULE</td>
</tr>
<tr>
<td>Min/Max Prop Delays</td>
<td>Pin Pairs</td>
<td>Not Applicable</td>
<td>PROPAGATION_DELAY</td>
</tr>
<tr>
<td>Min/Max Prop Delays</td>
<td>Min Delay</td>
<td>Not Applicable</td>
<td>PROPAGATION_DELAY</td>
</tr>
<tr>
<td></td>
<td>Max Delay</td>
<td>Not Applicable</td>
<td>PROPAGATION_DELAY</td>
</tr>
<tr>
<td>Total Etch Length</td>
<td>Minimum Total Length</td>
<td>Not Applicable</td>
<td>TOTALETCH_LENGTH</td>
</tr>
<tr>
<td></td>
<td>Maximum Total Length</td>
<td>Not Applicable</td>
<td>TOTALETCH_LENGTH</td>
</tr>
<tr>
<td>Relative Propagation Delay</td>
<td>Pin Pairs</td>
<td></td>
<td>RELATIVE_PROPAGATION_DELAY</td>
</tr>
</tbody>
</table>
### Table B-3  Routing Workbook

<table>
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<th>Worksheet</th>
<th>Column Heading</th>
<th>Cell Label</th>
<th>Property Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>Relative Propagation Delay (Continued)</td>
<td>Scope</td>
<td>RELATIVE_PROPAGATION_DELAY</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Delta Tolerance</td>
<td>RELATIVE_PROPAGATION_DELAY</td>
<td></td>
</tr>
</tbody>
</table>
Workbooks under the Net folder

Properties in the signal integrity workbook

Note: Constraint Manager, when launched from Allegro Designer, does not support the signal integrity workbook.

Table B-4 Signal Integrity Workbook

<table>
<thead>
<tr>
<th>Worksheet</th>
<th>Column Heading</th>
<th>Cell Label</th>
<th>Property Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>Electrical Properties</td>
<td>Frequency</td>
<td>Not Applicable</td>
<td>PULSE_PARAM</td>
</tr>
<tr>
<td></td>
<td>Period</td>
<td>Not Applicable</td>
<td>PULSE_PARAM</td>
</tr>
<tr>
<td></td>
<td>Duty Cycle</td>
<td>Not Applicable</td>
<td>PULSE_PARAM</td>
</tr>
<tr>
<td></td>
<td>Jitter</td>
<td>Not Applicable</td>
<td>PULSE_PARAM</td>
</tr>
<tr>
<td></td>
<td>Cycle to Measure</td>
<td>Not Applicable</td>
<td>PULSE_PARAM</td>
</tr>
<tr>
<td>Reflection</td>
<td>Overshoot</td>
<td>Max</td>
<td>MAX_OVERSHOOT</td>
</tr>
<tr>
<td>Edge Distortion</td>
<td>Edge Sensitivity</td>
<td>Sensitive Edge</td>
<td>EDGE_SENSE</td>
</tr>
<tr>
<td></td>
<td>First Incident Switch</td>
<td>Switch</td>
<td>FIRST_INCIDENT</td>
</tr>
<tr>
<td>Estimated Xtalk</td>
<td>Active Window</td>
<td>Not Applicable</td>
<td>XTALK_ACTIVE_TIME</td>
</tr>
<tr>
<td></td>
<td>Sensitive Window</td>
<td>Not Applicable</td>
<td>XTALK_SENSITIVE_TIME</td>
</tr>
<tr>
<td></td>
<td>Ignore Nets</td>
<td>Not Applicable</td>
<td>XTALK_IGNORE_NETS</td>
</tr>
<tr>
<td></td>
<td>Xtalk</td>
<td>Max</td>
<td>MAX_XTALK</td>
</tr>
<tr>
<td>Simulated Xtalk</td>
<td>Active Window</td>
<td>Not Applicable</td>
<td>XTALK_ACTIVE_TIME</td>
</tr>
<tr>
<td></td>
<td>Sensitive Window</td>
<td>Not Applicable</td>
<td>XTALK_SENSITIVE_TIME</td>
</tr>
<tr>
<td></td>
<td>Ignore Nets</td>
<td>Not Applicable</td>
<td>XTALK_IGNORE_NETS</td>
</tr>
<tr>
<td></td>
<td>Xtalk</td>
<td>Max</td>
<td>MAX_XTALK</td>
</tr>
<tr>
<td></td>
<td>Margin</td>
<td>Max</td>
<td>MAX_XTALK_MARGIN</td>
</tr>
<tr>
<td></td>
<td>Peak Xtalk</td>
<td>Max</td>
<td>MAX_PEAK_XTALK</td>
</tr>
<tr>
<td>SSN</td>
<td>Max SSN</td>
<td>Not Applicable</td>
<td>MAX_SSN</td>
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</table>
### Table B-4  Signal Integrity Workbook

<table>
<thead>
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<th>Worksheet</th>
<th>Column Heading</th>
<th>Cell Label</th>
<th>Property Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>SSN (Continued)</td>
<td>Power Bus Name</td>
<td>Not Applicable</td>
<td>MAX_SSN_POWER_BUS</td>
</tr>
<tr>
<td></td>
<td>Ground Bus Name</td>
<td>Not Applicable</td>
<td>MAX_SSN_GROUND_BUS</td>
</tr>
</tbody>
</table>

### Properties in the timing workbook

**Note:** Constraint Manager, when launched from Allegro Designer, does not support the timing workbook.

### Table B-5  Timing Workbook

<table>
<thead>
<tr>
<th>Worksheet</th>
<th>Column Heading</th>
<th>Cell Label</th>
<th>Property Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>Switch/Settle Delays</td>
<td>Min First Switch</td>
<td>Min</td>
<td>MIN_FIRST_SWITCH</td>
</tr>
<tr>
<td></td>
<td>Max Final Settle</td>
<td>Max</td>
<td>MAX_FINAL_SETTLE</td>
</tr>
<tr>
<td>Setup/Hold</td>
<td>Clock</td>
<td>Name</td>
<td>CLOCK_NET</td>
</tr>
<tr>
<td></td>
<td>Period</td>
<td></td>
<td>PULSE_PARAM</td>
</tr>
<tr>
<td></td>
<td>Jitter</td>
<td></td>
<td>PULSE_PARAM</td>
</tr>
<tr>
<td></td>
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## Properties in the routing workbook

### Table B-6 Routing Workbook

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