Design Synchronization and Packaging User Guide

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# Contents

## Preface
- About This Guide .......................................................... 9
- How To Use This Guide .................................................. 9
- Brief Outline of Different Chapters .................................. 10
- Related Documentation .................................................. 11

## 1 Introduction to the Design Synchronization Process
- Overview ................................................................................ 13
- Need for Synchronization ................................................... 14
- Design Synchronization Toolset ........................................... 14
  - Packager Setup ............................................................... 15
  - Packager Utilities ............................................................ 15
  - Design Differences .......................................................... 16
  - Design Association .......................................................... 17
  - Netrev .............................................................................. 17
  - Genfeedformat ................................................................. 17
- Front-to-back Flow .............................................................. 17
  - Overview ........................................................................... 17
  - Front-to-back Flow: Traditional Flow ............................... 19
  - Front-to-back: Constraint Manager Enabled Flow ............. 22
  - Design Synchronization Tasks .......................................... 25
- Getting Started with Design Synchronization ......................... 26
  - Overview ........................................................................... 26
  - Launching Design Differences ..................................... 26
  - Launching Design Association .................................. 27
  - Launching Packager Setup ............................................ 27
  - Launching Packager Utilities ..................................... 27
- Design Synchronization Process ........................................... 28
  - Defining Packager Setup Options .................................. 28
  - Packaging the Design .................................................. 28
Design Synchronization and Packaging User Guide

Running Packager Utilities ......................................................... 29
Exporting the Design ..................................................................... 29
Comparing the Schematic and the Layout ..................................... 31
Importing the Design ..................................................................... 32

2
Setting Up Packager-XL ................................................................. 35
Overview ....................................................................................... 35
Packager Setup Dialog Box ............................................................ 35
   Properties Tab ........................................................................... 37
State File Tab ................................................................................. 37
From Layout Tab ........................................................................... 37
Report Tab ...................................................................................... 38
Layout Tab ...................................................................................... 38
Subdesign Tab ................................................................................ 38
Changing the Packager Setup Properties ...................................... 39
   Adding and Deleting Properties .................................................. 41
Changing Packaging Information in the State File ....................... 42
   Overview of the State File .......................................................... 42
Changing the State File ................................................................. 43
Changing Feedback Properties in the Layout ............................... 46
Changing Packager Output Information ........................................... 48
Changing Reference Designators and Netlist Parameters ............ 51
Changing Setup Options While Packaging Subdesigns ............... 54

3
Allegro-Concept Property Flow ..................................................... 58
Overview ....................................................................................... 58
Allegro-Concept Property Flow Use Model ..................................... 58
Properties Flow from Allegro to Concept HDL ............................ 59
Opening the Property Flow Setup Dialog Box ............................... 60
Setting the Property Flow ............................................................. 63
   Adding New Properties .............................................................. 64
Deleting Properties ........................................................................ 65
Editing Properties ......................................................................... 65
4 Packaging Your Design .............................................................. 68

Overview ..................................................................................... 68
Where Packager-XL Fits in the PCB Design Process ......................... 69
Packager-XL Operation Modes ...................................................... 70
Forward Mode ............................................................................. 71
  Inputs in the Forward Mode ...................................................... 72
  Outputs From the Forward Mode ............................................... 73
Feedback Mode ............................................................................ 74
  Inputs to the Feedback Mode .................................................... 76
Properties and Directives .................................................................. 77
  Packager Properties .................................................................. 78
  Packager Directives .................................................................. 78
Prerequisites for Running Packager-XL ............................................. 79
Running Packager-XL in the Forward Mode ....................................... 79
  Updating the Board with the Changes in the Schematic ................. 79
  Using the State File for Successive Packager-XL Runs .................. 85
Running Packager-XL in the Feedback Mode ..................................... 86
  Overview ................................................................................. 86
  Updating the Schematic with the Changes in the Board ................. 86
  Using the pxlba.txt File for Controlling the Backannotation of Properties .................................................. 94
Packager-XL Exit Status .................................................................. 97
Using Packager Utilities ................................................................... 97
  Overview ................................................................................. 97
  Generating the Bill of Materials .................................................. 98
  Running Electrical Rule Checks ................................................ 100
  Generating Netlist Reports ......................................................... 101
  Viewing Any File .................................................................... 103
5
Resolving Design Differences ............................................. 104
  Overview ................................................................. 104
  How the Design Differences Tool Fits in the Front-to-Back Flow ............................................. 104
    Design Synchronization Flow: Constraint Manager Enabled Flow ............................................. 106
  Design Differences Functions ......................................... 108
  Running Design Differences ........................................... 108
  Design Differences User Interface .................................... 112
    Design Differences Toolbar ........................................... 112
    Design Differences Windows .......................................... 114
  Using Design Differences ................................................ 117
    Viewing Any Files ..................................................... 117
    Viewing the Logical Design ............................................ 118
    Viewing the Physical Design .......................................... 120
    Viewing the Differences in a Text Editor ............................................. 121
    Viewing Hierarchical Trees ............................................ 122
    Loading the Design Views ............................................. 124
    Querying a Design ...................................................... 125
    Highlighting and Dehighlighting Objects ............................................. 131
    Synchronizing Difference Views ...................................... 133
    Comparing Differences between Schematics and Boards ............................................. 137
    Filtering Differences Between Schematics and Boards ............................................. 141

6
Using Design Association .................................................. 144
  Overview ................................................................. 144
  How Design Association Fits in the Front-to-back Flow ............................................. 144
  Design Association Functions ........................................... 146
  Understanding Markers and Actions .................................... 146
  Launching and Exiting Design Association ............................................. 147
    Overview ................................................................. 147
    Launching from the Concept HDL Schematic ............................................. 147
    Launching from the Design Differences Tool ............................................. 147
    Exiting Design Association ............................................ 148
## Design Synchronization and Packaging User Guide

<table>
<thead>
<tr>
<th>Section</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Design Association User Interface</td>
<td>149</td>
</tr>
<tr>
<td>Main Window</td>
<td>150</td>
</tr>
<tr>
<td>Detail Window</td>
<td>151</td>
</tr>
<tr>
<td>Markers List Box</td>
<td>153</td>
</tr>
<tr>
<td>How Markers are Displayed</td>
<td>153</td>
</tr>
<tr>
<td>Execution Status of an Action</td>
<td>154</td>
</tr>
<tr>
<td>Action Types</td>
<td>154</td>
</tr>
<tr>
<td>Using Design Association</td>
<td>157</td>
</tr>
<tr>
<td>Displaying a Hierarchical Tree</td>
<td>158</td>
</tr>
<tr>
<td>Expanding a Marker</td>
<td>158</td>
</tr>
<tr>
<td>Starting an Action</td>
<td>159</td>
</tr>
<tr>
<td>Adding Locations, Nets, Instances, and Terminators</td>
<td>163</td>
</tr>
<tr>
<td>Backannotating to Concept HDL</td>
<td>166</td>
</tr>
<tr>
<td>Changing Parts</td>
<td>167</td>
</tr>
<tr>
<td>Opening and Saving the Markers File</td>
<td>172</td>
</tr>
</tbody>
</table>

## A

### Miscellaneous Items

<table>
<thead>
<tr>
<th>Section</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Logical View</td>
<td>174</td>
</tr>
<tr>
<td>Physical View</td>
<td>174</td>
</tr>
<tr>
<td>Sample propflow.txt File</td>
<td>174</td>
</tr>
<tr>
<td>List of Properties Filtered from Packager Files</td>
<td>175</td>
</tr>
</tbody>
</table>

## Index

<table>
<thead>
<tr>
<th>Section</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Index</td>
<td>178</td>
</tr>
</tbody>
</table>
Preface

About This Guide

The Design Synchronization and Packaging User Guide demonstrates the major features of the Design Synchronization solution, which is part of the front-to-back flow for PCB design. The Design Synchronization toolset lets you compare the logical design, that is, the schematic, and the physical design, that is, the board. You can update changes from the board to the schematic or from the schematic to the board. However, you cannot update changes across schematics or boards.

You can use the Design Synchronization and Packaging User Guide to perform the following tasks:

- Set the packaging options and package a design.
- Control the property flow between the schematic and the board.
- Synchronize the schematic and the board for any design. The guide details the functions of all tools in the Design Synchronization toolset. You learn about the procedures used in synchronizing the schematic and the board. You can synchronize the following differences:
  - connectivity differences
  - net differences
  - component differences
  - net property differences
  - pin property differences
  - component property differences.

How To Use This Guide

The Design Synchronization and Packaging User Guide contains the conceptual and procedural information necessary to use the Design Synchronization toolset. The organization of the user guide is based on how different tools in the Design Synchronization toolset are used to synchronize the schematic and the board. The first chapter explains the
design synchronization process. The subsequent chapters explain how to use the different Design Synchronization tools. See details in the Brief Outline of Different Chapters section.

If you are a new user and do not have any prior working experience with the Design Synchronization toolset, begin from the first chapter and continue learning about different tools in the sequence covered in the user guide. If you are using the user guide to find information about a design synchronization tool, you may directly refer to the chapter corresponding to a tool.

This guide assumes that you are familiar with the following tools in the front-to-back flow for PCB design:

- Project Manager
- Concept HDL
- Allegro

Brief Outline of Different Chapters

In Chapter 1, “Introduction to the Design Synchronization Process,” you will learn about the reasons for design synchronization. You will know about the functions of different tools in the Design Synchronization toolset. You will also learn about the important steps in the design synchronization process.

In Chapter 2, “Setting Up Packager-XL,” you will learn to set Packager-XL properties and directives. Packager-XL is a tool used to translate the schematic into the board and backannotate the changes made in the board to the schematic.

In Chapter 3, “Allegro-Concept Property Flow,” you will learn to control the flow of properties between Allegro and Concept HDL. By controlling the property flow, you have greater control in packaging a design. You can decide which properties should be packaged or backannotated.

In Chapter 4, “Packaging Your Design,” you will see the essential requirements to package a design. You will understand the difference between the Forward and Feedback mode for packaging a design. In the Forward mode, you package the schematic into the board. In the Feedback mode, you backannotate the changes from the board to the schematic. In this chapter, you will also learn to create netlists and synchronize the changes between the board and the schematic.

In Chapter 5, “Resolving Design Differences,” you will use the Visual Design Differences (VDD) tool to view the differences between the schematic and the board. You will also learn
to filter specific differences, and update a specific difference or all differences in either the schematic or the board.

In Chapter 6, “Using Design Association,” you will use the Design Association tool to synchronize the connectivity changes between the schematic and the board. You will be able to identify the different types of markers and use them to synchronize the schematic and the board.

Related Documentation

You can use the Design Synchronization and Packaging User Guide to use Visual Design Differences (commonly referred to as Design Differences), Design Association, and Packager Setup. To see information about the commands and the associated tasks related with the dialog boxes of the Design Synchronization toolset, see Design Synchronization Online Help.

The Design Synchronization and Packaging User Guide introduces the basic concepts of packaging a design. For more detailed description of the packaging process and how you can optimize it, see the Cadence document Packager-XL Reference.

If you want to learn by doing, see the Cadence document Design Synchronization Tutorial. This tutorial includes a design example and step-by-step instructions that are useful to practice synchronizing boards and schematics.
Introduction to the Design Synchronization Process

Overview

The development of any design requires synchronization between the schematic and the board. Based on how you prepare a new design, you can synchronize the schematic and the board in one of the following two ways:

1. The conventional or linear flow

   In the conventional flow, you first design the schematic, make changes to it, get the schematic reviewed and approved. Next, you prepare the board and send it for manufacturing. When you prepare the board, last-minute changes, such as adding termination resistors or removing certain components, can cause property changes and connectivity differences between the schematic and the board. These changes need to be backannotated to the schematic.

2. The parallel flow

   In the parallel flow, the schematic designers and board designers work in parallel. First, the schematic designer starts work on the schematic. At a logical point, the board designer imports the schematic and uses it to create the board. Meanwhile, the schematic designer starts work on the next module. At the next logical point, the schematic designer might add some new information to the schematic and the board designer might make changes to the board that require backannotation to the schematic. Therefore, it is important to synchronize the schematic and the board.

Whether you follow the linear flow or the parallel flow, it is important that the schematic and the board are always synchronized. The process of synchronizing the schematic and the board is called design synchronization. You can use the Design Synchronization toolset to synchronize differences between the schematic and the board.
Need for Synchronization

The primary need for synchronization is caused by changes that occur either in the board or in the schematic after the initial transfer of packaged information to the board.

The following four changes occur in the board after the initial transfer of packaged information from the schematic:

1. Component changes
   You might add new components in the design to handle signal integrity and electromagnetic compatibility problems. These components can include termination resistors, series or shunt buffers, and bypass capacitors.

2. Connectivity changes
   You might make connectivity changes to facilitate routing after the initial placement of components. Connectivity changes might be caused by pin swaps, section swaps, and reference designator (refdes) swaps.

3. Reference designator changes
   You might change the reference designators to debug board problems.

4. Property changes
   You might modify certain components in the board. These modifications will cause property changes.

Besides the changes in the board after the initial transfer of packaged information from the schematic, certain changes, such as Engineering Change Order (ECO), are also made in the schematic. The need for the Design Synchronization toolset arises from the need to synchronize the above-mentioned differences between the schematic and the board.

Design Synchronization Toolset

The Design Synchronization toolset includes the following tools:

- Packager Setup
- Packager Utilities
- Design Differences
- Design Association
- Netrev
Packager Setup

The Packager Setup tool is used to view or change the default packaging setup options in the project file. By controlling the default packaging options, you can define the properties that must be packaged or backannotated. You can also control the reports that you want to generate while packaging a design.

Packager utilities and Design Differences follow the Packager Setup options of the project file. You can change the Packager settings in the Packager Setup tool and thereby control how the design is packaged.

Note: The word Packager represents Packager-XL. Packager-XL is the interface between the logical design (schematic) and the physical layout (board) in the Cadence Board Design Solution.

Packager Utilities

There are five Packager utilities.

- Export Physical
- Import Physical
- BOM
- Electrical Rule Check
- Netlist Reports

Export Physical

Export Physical translates a logical design entered in Concept HDL into a physical design ready for layout. For more information about translating a logical design into a physical design, refer to Exporting the Design on page 29.

Import Physical

Import Physical receives property/swapping changes made in Allegro and incorporates them into the logical design. See Importing the Design on page 32 for more information about feeding back the changes made in a board to the schematic.
BOM

The BOM (Bill of Material) utility creates BOM reports that are useful for manufacturing. You can use the BOM-HDL tool to generate BOM reports in multiple formats such as text, spreadsheet, and HTML. BOM-HDL supports standard templates that display BOM reports in a user-friendly manner. Besides, you can create new templates to customize the report. See Generating the Bill of Materials on page 98 for more information about generating BOM reports.

Electrical Rule Check

The Electrical Rule Check utility helps you check for compatible outputs, single-node nets, source/driver checks, net loading, and pin directions. The utility generates a summary of electrical rule violations in a report named `erc.rpt`. See Running Electrical Rule Checks on page 100 for more information about performing electrical rule checks.

Netlist Reports

The Netlist Reports utility prepares different types of netlist reports. See Generating Netlist Reports on page 101 for more information about generating netlist reports.

Design Differences

The Design Differences tool (also referred to as Visual Design Differences or VDD) compares the schematics and boards and generates a list of differences. VDD displays these differences in difference view windows. VDD records the following:

- Differences in instances, nets, and pin connectivity.
- Differences in properties on instances, nets, and pins.
- Information about function and pin swaps.
- Information about reference designator renames.

VDD supports various controls to view, query, and filter the differences between the schematic and the board. You can update either the schematic or the board by accepting or rejecting individual differences. You can even accept or reject all differences simultaneously.
Design Association

Design Association (DA) is used to update the connectivity changes made in the board to the schematic. To update the connectivity changes, Design Association requires the dessync.mkr file produced by the Design Differences tool.

Netrev

Netrev is a tool that loads the packager output into a database for the physical layout. This database works as the board file, which is operated on by Allegro or SPECCTRAQuest.

Genfeedformat

Genfeedformat extracts connectivity and property information from the board into view files that are used by Design Differences and Packager-XL.

Front-to-back Flow

Overview

Traditionally, before the release of Design Synchronization tools, the conventional front-to-back flow worked as depicted in the Figure 1-1 on page 18.
1. Create schematic files by using a schematic editor such as Concept HDL.

2. Package the design into Packager-XL files. Three files \( \text{pstchip.dat}, \text{pstxprt.dat}, \) and \( \text{pstxnet.dat} \) are generated.

3. Use netrev to take the Packager-XL files to the board.

4. Feed back the property changes to the schematic by generating the feedback files \( \text{pinview.dat}, \text{netview.dat}, \text{funcview.dat}, \text{and compview.dat} \) and use these files to create Packager-XL backannotation files to backannotate the schematic.

While the conventional flow was able to successfully transfer property changes made in the board back to the schematic, it could not highlight connectivity changes to the schematic. The conventional front-to-back flow did not have any tool that could capture the connectivity.
changes in the board and feed them back to the schematic. The use of the Design Synchronization toolset helped overcome the problem of synchronizing the connectivity changes between the schematic and the board.

**Front-to-back Flow: Traditional Flow**

The enhanced front-to-back flow from Version 13.6 (traditional flow in the context of Version 14.2) lets you compare the schematic and board information by comparing the Packager-XL files and the feedback files generated from the board. The Front-to-back: Traditional Flow figure on page 20 displays the enhanced flow.

This flow represents the front-to-back flow with Constraint Manager disabled. Electrical constraints are treated as properties.

**Note:** Constraint Manager allows you to manage electrical constraints in a design. Front-to-back: Constraint Manager Enabled Flow on page 22 covers how the Design Synchronization flow changes when Constraint Manager is used to manage electrical constraints.

**Caution**

*You cannot mix between two flows. If you select the Constraint Manager enabled flow, you cannot move back to the traditional flow.*

When running in the traditional flow, Packager-XL produces 3 files containing packaging information:

- **pstchip.dat**—Contains a physical description for each physical part used in your design. Packager-XL extracts this physical description from chips files, ptf files, and properties on schematic instances. This file contains a description of only the physical parts used in the design.

- **pstxprt.dat**—Lists each reference designator and the sections assigned to it.

- **pstxnet.dat**—The pstxnet.dat file is the connectivity file. This file lists each net, its properties, its attached nodes, and node properties. The list is ordered by physical net name and contains all net properties and the logic-to-physical binding of nets and nodes.

These files are used by Netrev to create or update the board database. You can run Netrev from Export Physical or Allegro (*File > Import > Logic*).
Figure 1-2  Front-to-back: Traditional Flow

Start here

Concept HDL

Packager-XL (Export Physical)

Netrev

Allegro or SPECCTRAQuest

Design Association

Design Differences

Packager-XL (Import Physical)

Genfeedformat

Schematic

Property changes / backannotation

Forward Flow

Backward flow

Inputs for Design Differences

Backfind format

Feedback files (4 *view.dat files)

PXL files (3 pst*.dat files)

Board files

PXL files (*view.dat)

Dessync.mkr

Backannotate changes

Connectivity changes

Front End

Front-to-Back

Back End

1

2

3
You can make changes in Allegro and then feed back the changes in the board to the schematic by generating the feedback files using genfeedformat. You can run genfeedformat from Import Physical or Allegro. The following files are generated by genfeedformat:

- **pinview.dat**—Contains connectivity and pin instance properties info generated by Allegro
- **netview.dat**—Contains property information for the nets generated by Allegro
- **funcview.dat**—Contains property information for the schematic instances generated by Allegro
- **compview.dat**—Contains property information for the component instances generated by Allegro

You can now use the feedback files to synchronize the schematic and the board by doing one of the following:

- Run Import Physical to read the changes made in Allegro and update the schematic. You can directly backannotate all changes in the board to the schematic from Import Physical or you can choose *Tools > Back Annotate* in Concept HDL to backannotate all the changes in the board to the schematic.

- Use the Design Differences (VDD) and Design Association (DA) tools to resolve individual connectivity and property differences between the schematic and the board. Use VDD to update the property differences either to the board or to the schematic. When you run VDD, it displays differences in properties between the schematic and the board in multiple difference view windows.

**Note:** See *Differences View Windows: Traditional Flow* on page 114 for more information about difference windows.

Use DA to update the connectivity changes made in the board to the schematic. DA uses a file generated by VDD named *dessync.mkri* (which captures connectivity information) to guide you in updating the schematic. If you have made connectivity changes in the schematic, then you need to run Export Physical to push these changes to the board.

**Note:** While the Design Synchronization toolset helps you synchronize logical-to-physical design differences, it does not allow you to synchronize logical-to-logical or physical-to-physical differences. This implies that you cannot synchronize two schematics or two boards with the Design Synchronization toolset.

You can use the Property Flow Setup dialog box to define the properties that should be transferred between the board and the schematic. The improved property flow allows Design Differences to have a smoother run as it has to capture fewer property mismatches. See *Allegro-Concept Property Flow* on page 58 for more information about setting the property flow.
Front-to-back: Constraint Manager Enabled Flow

The primary difference between design synchronization flow in the traditional flow and Constraint Manager enabled flow is the use of Constraint Manager for managing electrical constraints in Concept HDL. If you use Constraint Manager in Concept HDL to manage electrical constraints, then Constraint Manager dumps information about electrical constraints in a new view named constraints under the root design. This view includes a file named <root_design>.dcf, which contains a snapshot of electrical constraint information in the design.

Important

If you are using the Constraint Manager enabled flow:

- You must not use Concept HDL 14.2 with Allegro or SPECCTRAQuest 14.1 or earlier versions.
- You must not use Concept HDL 14.1 or a previous version with Allegro or SPECCTRAQuest 14.2.
Figure 1-3 Front-to-back: Constraint Manager Enabled Flow

Start here

Concept HDL

Constraint Manager

Schematic

<root_design_name.dcf> file

Packager-XL (Export Physical)

PXL files (5 pst*.dat files)

Netrev

Design Association

Design Differences

Packager-XL (Import Physical)

Genfeedformat

Allegro or SPECCTRAQuest

Forward Flow

Backward flow

Inputs for Design Differences

Board files

Backannotate changes

Connectivity changes

Property changes / backannotation

Feedback files (6 *view.dat files)

PXL files (*view.dat)

Dessync.mkr

Front End

1

Front-to-Back

2

Back End

3
In the Constraint Manager enabled flow, Packager-XL creates five `pst*.dat` files when you run Export Physical (with Package Design and Update Allegro Board (Netrev) check boxes selected). These include the three files generated in the traditional flow (`pstchip.dat`, `pstmprt.dat`, and `pstxnet.dat`) and the following two files:

- **`pstcmdb.dat`**—Contains definition of electrical constraints in the schematic as defined and created in the Constraint Manager database. This file is a copy of the `<design_name>.dcf` file in the constraints view, where `<design_name>` represents the name of the root cell of the schematic, and the dcf extension signifies that the file is a constraint file.

  **Note:** In the traditional flow, information about electrical constraints on the schematic is stored in the `pstxnet.dat` file. In the Constraint Manager enabled flow, information about electrical constraints on the schematic is stored in the `pstcmdb.dat` file and not in the `pstxnet.dat` file.

- **`pstmcbc.dat`**—Contains the electrical constraint baseline information in the schematic data. This file is a copy of the `<design_name>.dcf,p` file in the constraints view. When the first time Constraint Manager is invoked or the Export Physical is run, the `<design_name>.dcf,p` file is generated.

  **Note:** If the `<root_design_name>.dcf` file is not present, Packager-XL runs in the traditional flow, where the information about electrical constraints are passed as normal properties in the `pstxnet.dat` file.

The five `pst*.dat` files are used by Netrev to create or update the board. You can make changes in Allegro and then feed back the changes in the board to the schematic by running Import Physical (with Generate Feedback Files check box, Package Design check box and Allegro option selected). Import Physical allows you to overwrite all current electrical constraints in the schematic with the electrical constraint information in the Allegro board file or import only the electrical constraint information that has changed in the Allegro board file since the last import. Import Physical detects the presence of the `<root_design_name>.dcf` file and runs in the Constraint Manager enabled flow.

**Note:** If the `<root_design_name>.dcf` file exists in the constraints view of the root design, you are using the Constraint Manager enabled flow. The Extract Constraints check box in the Import Physical dialog box will be selected by default. You cannot clear this check box because once you are in the Constraint Manager enabled flow, you cannot go back to the traditional flow.

When you run Import Physical, `genfeedformat` creates the following six feedback files—`pinview.dat`, `netview.dat`, `funcview.dat`, `compview.dat`, `cmdbview.dat`, and `cmbcview.dat`. Note that the first four files are the same as those created in the traditional flow. The remaining two files contain electrical information as described below:

- **`cmdbview.dat`**—Describes the current electrical constraint information for the design.
Design Synchronization and Packaging User Guide
Introduction to the Design Synchronization Process

- **cmbcview.dat**—Specifies the base copy of the electrical constraint information used by the Allegro board snapshot.

You can now use the feedback files to synchronize the schematic and the board by doing one of the following:

- Choose **Tools > Back Annotate** in Concept HDL to backannotate all the changes in the board to the schematic. Select the **Package Backannotation** check box in the **Backannotation** dialog box to backannotate all changes (excluding changes in electrical constraint information) in the board to the schematic. Select the **Constraint Backannotation** check box in the **Backannotation** dialog box to backannotate changes in electrical constraint information in the board to the schematic.

- Use the Design Differences (VDD) and Design Association (DA) tools to resolve individual connectivity and property differences between the schematic and the board.

  Use VDD to update the property differences either to the board or to the schematic. When you run VDD, it displays differences in properties between the schematic and the board in multiple windows. The differences in electrical constraints information in the schematic and the board are displayed in two difference windows—**Constraints Differences-Logical** and **Constraints Differences-Physical**. See **Differences View Windows: Traditional Flow** on page 114 for more information about these windows.

  **Note:** In the traditional flow, differences in electrical constraints between the schematic and the board are displayed in the **Net Property Difference** window.

  Use DA to update the connectivity changes made in the board to the schematic. DA uses a file generated by VDD named **dessync.mkr** (which captures connectivity information) to guide you in updating the schematic.

  The behavior of DA is the same regardless of whether you run it in the Constraint Manager enabled flow or the traditional flow.

**Design Synchronization Tasks**

The entire Design Synchronization process can involve the following tasks:

1. Package and export the Concept HDL schematic design to the Allegro or SPECCTRAQuest layout by running Packager-XL in the Forward mode. Use Export Physical to package the design.

2. Compare the schematic and layout designs by using the Design Differences tool.

3. Package the design for feedback by running Packager-XL in the Feedback mode.
4. Generate the `dessync.mkr` marker file to backannotate the physical connectivity changes to the Concept HDL schematic by using the Design Association tool.

5. Backannotate the schematic based on information in the board.

6. Run the Packager utilities to complete any or all of the following steps:
   - a. Generating the Bill of Materials
   - b. Performing electrical rule checks
   - c. Generating netlist reports

7. Run Packager Setup to complete any or all of the following steps:
   - a. Viewing the default Packager Setup options
   - b. Changing the default Packager Setup options

### Getting Started with Design Synchronization

#### Overview

Depending on the task to execute, you can launch one of the following tools:

- Design Differences
- Design Association
- Packager-XL
- Packager utilities (Bill of Materials, Electrical Rules, Netlist Rules, Export Physical, and Import Physical)

You can launch these tools from either the Project Manager user interface or the Concept HDL schematic editor.

#### Launching Design Differences

You can launch Design Differences in one of the following three ways:

- Click the Design Sync icon in Project Manager. A drop-down list appears. Select the Design Differences option from the list.
- From Project Manager, choose Tools - Design Sync - Design Differences.
From Concept HDL, choose Tools - Design Differences.

### Launching Design Association

Before you launch the Design Association tool, ensure the following:

- You have expanded the design in the Concept HDL editor. A warning message to expand the design is displayed if you launch the Design Association tool without expanding the Concept HDL design.
- You have run the Design Differences tool and generated the dessync.mkr marker file. This file is used by Design Association to synchronize connectivity differences.

To launch Design Association:

➢ From the Concept HDL menu bar, choose Tools - Design Association.

### Launching Packager Setup

You can launch Packager Setup in one of the following two ways:

1. Click Advanced in the Export Physical or Export To Packager Files dialog box.
2. Click Options in the Import Physical, Design Differences, or Import From Feedback Files dialog box.

### Launching Packager Utilities

You can launch Export Physical and Import Physical utilities from Project Manager in one of the following two ways:

1. Click the Design Sync icon.
2. Choose Tools - Design Sync, and click on the Export Physical or Import Physical option in the drop-down menu.

To launch other Packager utilities such as Bill of Materials, Electrical Rules, and Netlist Reports, complete the following step:

➢ Choose Tools - Packager Utilities, and click the appropriate option.
Design Synchronization Process

The following are the key procedures in the Design Synchronization process:

- Define Packager-XL setup options.
- Package the design.
- Run Packager utilities.
- Export the design.
- Compare the schematic and the layout.
- Import the design.

Defining Packager Setup Options

The Packager Setup tool helps you record the default packaging setup options in the project file. The Export, Import, Design Differences, Package, and Feedback commands use the default packaging settings in the project file to complete their operations.

You can use Packager Setup to change the information about properties and define how to package them. For example, you can use Packager Setup to change the properties that will be packaged in the Forward and Feedback modes. You can also use the Packager Setup tool to define how Packager-XL formats output reports. See Setting Up Packager-XL on page 35 for more information about the different Packager Setup options and how to change them.

Packaging the Design

Packaging involves converting a logical design into a physical layout and vice versa. The tool that completes packaging is Packager-XL. Packager-XL works in the following two modes:

- Forward Mode
  Packager-XL translates a logical design entered in Concept HDL into a physical design ready for layout on Allegro.

- Feedback Mode
  Packager-XL receives the changes made in the physical design in Allegro and incorporates these changes into the logical board.

See Packaging Your Design on page 68 for more information about packaging a design.
Running Packager Utilities

There are three packager utilities: the BOM utility, the Electrical Rules utility, and the Netlist Reports utility. Using these utilities, you can generate the Bill of Material reports, run electrical rule checks on the design, and generate netlist reports.

See Packaging Your Design on page 68 for more information about the Packager utilities.

Exporting the Design

The Export Physical command transfers the Concept HDL schematic to the physical Allegro layout database. To run this command, you use the Export Physical dialog box.

Depending on the presence of the <root_drawing>.dcf file in the constraints view, Export Physical runs in 2 flows, traditional flow and Constraint Manager enabled flow. See Running Packager-XL in the Forward Mode on page 79 for more information about running Export Physical in different flows.
Figure 1-4 Export Physical Dialog Box

Click OK in the Export Physical dialog box to run the Export Physical command.

The Export Physical command performs the following tasks:

- Expands and packages the schematic design by using Packager-XL (if you have selected the Package Design option and defined the packaging options)
- Transfers the schematic design to the Allegro layout by using the netrev program
- Transfers information about electrical constraints to Allegro and updates the physical Allegro or SPECCTRAQuest layout board with the latest logical schematic data
- Backannotates the latest packaged and constraint information to the schematic
Introduction to the Design Synchronization Process

See Packaging Your Design on page 68 for more information about exporting a design.

Comparing the Schematic and the Layout

A design and a board are “in sync” when they represent the same logical circuit, have identical packaging, and share the same set of properties. They get “out of sync” when changes are made to the board or the schematic.

The Design Differences command finds differences between the board (physical data in the Allegro or SPECCTRAQuest layout) and the schematic (logical data in the Concept HDL schematic) when they are “out of sync”. To run the Design Differences command, you use the Design Differences dialog box. Design Differences may run in 2 flows, traditional flow and Constraint Manager enabled flow.

- **Traditional flow**: This is the default flow. In this flow, Design Differences does not distinguish electrical properties differences from other properties and displays the differences between the schematic and the board in the net and properties difference windows.

  The traditional flow is selected when `<root_drawing>.dcf` file is not found in the constraints view and none of the `pstmdb.dat` or `cmbcv.dat` or `cmdbview.dat` files are present in the packaged view.

- **Constraint Manager enabled flow**: In this flow, Design Differences displays constraint differences in 2 new Constraints Differences windows, one each for logical and physical domain. Any constraint property differences are filtered from the net-properties difference windows and displayed in the new windows.

  **Note**: See Differences View Windows: Constraint Manager Enabled Flow on page 115 for more information about Constraints Differences windows.

  The Constraint Manager enabled flow is selected when `<root_drawing>.dcf` file is found in the constraints view or the `pstmdb.dat` or `cmbcv.dat` or `cmdbview.dat` files are present in the packaged view.

The Design Differences Dialog Box: Traditional Flow figure on page 32 shows Design Differences in the traditional flow.
Design Synchronization and Packaging User Guide
Introduction to the Design Synchronization Process

Figure 1-5  Design Differences Dialog Box: Traditional Flow

➤ Click OK in the Design Differences dialog box to run the Design Differences command.

Note: See Design Differences Functions on page 108 for more information about comparing the schematic and the layout and resolving design differences.

The design differences command performs the following tasks:

- Calls Export Physical to package the design
- Extracts the design from Allegro
- Generates design differences
- Displays the Design Differences user interface

Importing the Design

The Import Physical command transfers the physical design from the Allegro or SPECCTRAQuest layout database to the Concept HDL schematic. To run the Import Physical command, use the Import Physical dialog box.

Depending on whether Constraint Manager has been used in Concept HDL and the selection of the Extract Constraints check box, import physical runs in 2 flows, traditional and Constraint Manager enabled flow. See Running Packager-XL in the Feedback Mode on page 86 for more information about running Import Physical in different flows.
Click **OK** in the Import Physical dialog box to run the **Import Physical** command.

The **Import Physical** command performs the following tasks:

- Runs the Allegro extract program and generates feedback files using the Genfeedformat tool.
- Processes the electrical constraint feedback files (*cmdbview.dat* and *cmbcview.dat*) generated from Allegro and updates the constraints view of the design.
- Runs Packager-XL in the Feedback mode and packages the physical design.
- Backannotates all the changes (electrical, connectivity, and constraints) made in the board to the schematic.

**Note:** In the Constraint Manager enabled flow, Import Physical in addition to the above steps will generate electrical constraint backannotation files. Packager-XL also extracts the constraints differences in the board to a file called *pstcmback.dat*. 
If you do not backannotate the changes using Import Physical, you can use one of the following two operations to transfer the physical design changes from the layout database to the Concept HDL schematic:

- Choose Tools - Backannotate in the Concept HDL menu bar to feedback the changes from the layout to the schematic.
- Use the Design Association tool to feedback the connectivity changes from the layout to the schematic.

If you do not have access to Allegro or the Allegro layout (*.brd file), but have access to the feedback files, you can use them to feedback the physical design from the layout and backannotate the changes made in the layout to the design.

Feeding back involves generating the feedback files from the Allegro layout and packaging the design with the feedback files. To feedback to the design:

1. Choose Design Sync - Import Physical to launch the Import Physical dialog box.
2. Click OK to start the Feedback command.

By default, both the Generate Feedback Files option and the Package Design (Feedback) option are selected in the Import Physical dialog box. Therefore, if you click the OK button without changing any selection, Packager-XL generates the feedback files and packages the design for feedback.
Setting Up Packager-XL

Overview

The Packager Setup tool is used to view or change the default packaging options in the project file. Packager utilities and Design Differences obtain their Packager Setup options from the project file. You can use Packager Setup to define how a design will be packaged.

Packager Setup Dialog Box

To change any Packager Setup option, you use the Packager Setup dialog box. To launch the Packager Setup dialog box, refer to Launching Packager Setup on page 27.

Note: Depending on how you launch the Packager Setup dialog box, the available packaging options vary. If you launch Packager Setup from the Project Setup dialog box, the titlebar of the Packager Setup dialog box will display the name Project Setup. This dialog box contains all the options supported by Packager Setup. It also contains some additional options such as Optimize and Repackage.
Figure 2-1  Packager Setup Dialog Box

The Packager Setup dialog box contains six tabs:

- Properties Tab
- State File Tab
- From Layout Tab
- Report Tab
- Layout Tab
- Subdesign Tab
Each tab controls a group of Packager settings. To view or change the default Packager Setup options, you can select any of these tabs.

**Properties Tab**

The *Properties* tab is the default tab. You use this page to package schematic instances that share the same properties. You can create component definition properties, that is, the properties for which Packager-XL creates alternate physical parts. You can also create filters that specify the properties that must not be packaged. You can specify the properties listed in the Packager output files. Finally, you can use the *Property Flow Setup* button to launch the Property Flow Setup dialog box, which helps you to set the default properties that flow between Concept HDL and Allegro.

See *Changing the Packager Setup Properties* on page 39 for more information.

**State File Tab**

You can use the *State File* tab to control the properties in the state file. The state file is used to store a flattened, packaged view of the design. It contains all the packaging properties used in the design, the physical net names, and the properties whose values differ from those in the schematic. Using the *State File* tab, you can define the properties in the state file that replace the corresponding properties in the schematic. You can also define the properties that will replace the properties in the layout file (in case of differing values). Finally, you can use the *State File* tab to remove properties from the state file.

**Note:** When you remove properties from the state file, the properties in the schematic or the layout automatically win.

See *Changing Packaging Information in the State File* on page 42 for more information.

**From Layout Tab**

You can use the *From Layout* tab to control the properties that will be fed back or backannotated from the layout to the schematic. You can specify whether or not a particular property will be backannotated.

See *Changing Feedback Properties in the Layout* on page 46 for more information.
Report Tab

You can use the *Report* tab to specify the Packager-XL output. By default, Packager-XL generates a number of report files. You can also select the report files that you need as output. For more information about Packager-XL report files, see *Packaging Your Design*.

You can also use the *Report* tab to control the display of warnings when Packager-XL packages a design. By default, all warnings are displayed. You can suppress any warning.

See *Changing Packager Output Information* on page 48 for more information.

Layout Tab

You can use the *Layout* tab to modify layout netlist parameters and reference designators. You can change reference designator naming schemes. You can also change the default prefix for reference designators. You can increase or decrease the number of characters used to define component or physical net names. Finally, you can define which characters can or cannot be used in defining net names.

See *Changing Reference Designators and Netlist Parameters* on page 51 for more information.

Subdesign Tab

You can use the *Subdesign* tab to specify how to package blocks in hierarchical designs. You can generate a specific subdesign state file for the block. After defining a subdesign state file, you can force packaging to each instance of the subdesign in the subdesign state file. You can even customize how packaging in the subdesign state file is used in place of new subdesign instances.

See *Changing Setup Options While Packaging Subdesigns* on page 54 for more information.

**Caution**

*When changing the default Packager Setup options. Unless you are sure that the change you require is necessary, do not change the default settings.*
Changing the Packager Setup Properties

To change the default properties that will be used by Packager-XL, use Packager Setup - Properties Tab.

Figure 2-2 Packager Setup - Properties Tab

You can make seven types of property changes by using the Properties tab.

1. Make packages.

A package consists of schematic instances that share properties with the same value. Packager-XL does not package together any instances that have different values for the
same property. You can define packages by adding properties in the Package list box. For more information about adding or removing properties in the Package list box, see Adding and Deleting Properties.

**Note:** The packaged properties are assigned the `PACKAGE_PROP` directive.

For more information about the `PACKAGE_PROP` directive, see the Cadence document Packager-XL Reference.

2. Create strict packages.

A strict package is used to restrict the packaging of schematic instances. A strict package includes only the instances with the package properties. You cannot package any other properties in a strict package. You can define strict packages by adding properties in the Strict Package list box.

**Note:** Strict packages are defined using the `STRICT_PACKAGE_PROP` directive. See the Cadence document Packager-XL Reference for more information about the `STRICT_PACKAGE_PROP` directive.

3. Define component definition properties.

Component definition properties are used by Packager-XL to create alternate physical parts. To define these properties, add them in the Component Definition list box.

**Note:** Component definition properties are defined using the `COMP_DEF_PROP` directive. See the Cadence document Packager-XL Reference for more information about the `COMP_DEF_PROP` directive.

4. Define component instance properties.

You can use the Properties tab to define the properties that will be treated as component instance properties. Packager-XL creates alternate physical parts for component instance properties. To define these properties, add them in the Component Instance list box.

**Note:** Component instance properties are defined using the `COMP_INST_PROP` directive. See the Cadence document Packager-XL Reference for more information about the `COMP_INST_PROP` directive.

5. Define the properties that be filtered from the `pstprop.dat` file.

To filter a conflicting property from the `pstprop.dat` file, you can add it to the Property Conflicts Filter list box.

6. Filter properties.

To omit any property from the packager output files, you can add them to the Filter list box.
Note: The FILTERPROPERTY directive is used to filter out properties from the packager output files. See the Cadence document Packager-XL Reference for more information about the FILTERPROPERTY directive.

7. Pass properties to the packager output files.

To pass any property to the packager output files, you can add it to the Pass list box.

Note: The PASSPROPERTY directive is used to pass properties to the packager output files. See the Cadence document Packager-XL Reference for more information about the PASSPROPERTY directive.

8. Change the default property flow between Concept HDL and Allegro.

Click the Property Flow Setup button to launch the Property Flow Setup dialog box. You can use the Property Flow Setup dialog box to add, edit, or remove properties that flow between Concept HDL and Allegro. You can even change the property flow by importing properties from the pxlba.txt file and packaged files.

After you have added or removed properties, check if you need to change any other setup options in the other five tabs. To change information in another tab, select that tab and make the required changes. You can click the OK button to accept the changes, or click the Cancel button to ignore the changes.

If you have made any property changes in the current session and want to ignore the changes, click the Reset button.

Adding and Deleting Properties

Adding a Property

1. To add a property to any list in the Packager Setup dialog box, click the Add button corresponding to that list.

   The Add Property dialog box appears.
Figure 2-3  Add Property Dialog Box

2. To add the property, type its name in the Property Name list. You can also select a name from the Property Name list.

3. Click OK to add the property.

Removing a Property

1. Select the property to be removed in the Packager Setup dialog box.

2. Click the Remove button.

Changing Packaging Information in the State File

Overview of the State File

The state file is used to store a flattened, packaged view of the design. It contains all the packaging properties used in the design, physical net names, and the properties whose values differ from those in the schematic. By default, Packager-XL uses the information in the state file to maintain the existing packaging assignments. If you do not want to use the existing packaging assignments, set the REPACKAGE directive to on. For more information about the REPACKAGE directive, see the Cadence document Packager-XL Reference.

The STATE_WINS_OVER_DESIGN and STATE_WINS_OVER_LAYOUT directives are used to control the precedence of properties in the schematic, layout, and state file. You can set these directives from the State File tab in the Packager Setup dialog box.

The STATE_WINS_OVER_DESIGN directive specifies whether or not the property values in the state file will replace the schematic values. The default value is off. This value specifies
that the schematic property values take precedence over the values in the state file. To preserve the changes made during the layout phase, you need to complete one of the following tasks:

- Backannotate your schematic after running Packager-XL in the Feedback mode.
- Set the `STATE_WINS_OVER_DESIGN` directive to `on`.

**Note:** It is recommended that you backannotate your design after packaging in the Feedback mode and let the `STATE_WINS_OVER_DESIGN` directive remain `off`.

If you want the feedback values in the state file to replace any values in the schematic, set the `STATE_WINS_OVER_DESIGN` directive to `on`. This setting preserves the property values fed back from the layout. Consequently, the schematic does not display the values used by Packager-XL and any changes to the packaging properties in the schematic are ignored.

The `STATE_WINS_OVER_LAYOUT` directive specifies whether or not the property values in the state file will replace the feedback values (that is, the changes made in the layout). The default value is `off`. It specifies that the feedback values take precedence over the values in the state file.

**Note:** By setting the `STATE_WINS_OVER_LAYOUT` directive to `on`, you force the packaging changes to originate in the schematic. The property values in the state file will not replace the property values in the schematic. The value `on` for the `STATE_WINS_OVER_LAYOUT` directive might prove too restrictive. It is recommended that you let the `STATE_WINS_OVER_LAYOUT` directive remain `off`.

### Changing the State File

To change the packaging information in the state file, select the *State File* tab.
You can use the *State File* tab to make the following changes:

1. Change the properties in the state file.

   You can use the *Remove From State* group box to remove properties from the state file. Packager-XL cannot reuse existing packaging information for the properties that are removed from the state file. Therefore, you must be cautious while removing properties from the state file.

   If you want to remove all the properties from the state file, click the *All Properties* radio button.
To remove specific properties from the state file, select the Specific Properties radio button and remove properties. See Adding and Deleting Properties for more information about adding or removing properties from the Remove From State list box.

**Note:** The REMOVE_FROM_STATE directive is used to remove properties from the state file. For more information about the REMOVE_FROM_STATE directive, see the Cadence document Packager-XL Reference.

2. Define the properties in the state file that replace the properties in the design.

By default, the properties in the schematic always replace the properties in the state file. However, you can define the properties in the state file that will replace similar properties in the schematic. If you want to make all properties in the state file, replace the properties in the schematic, select the All Properties radio button.

To make specific properties in the state file replace the schematic properties, select the Specific Properties radio button and add or remove properties. See Adding and Deleting Properties for more information about adding or removing properties from the State Wins Over Design list box in the Packager Setup dialog box.

To revert to the default selection, where the schematic properties will always replace the state file properties, select the Never radio button.

3. Define the properties in the state file that replace the properties in the layout.

By default, the properties in the state file never replace the feedback values in the layout. However, you can define the properties in the state file that replace the properties in the layout. If you want to make all properties in the state file, replace the properties in the layout, select the All Properties radio button. This is the default selection.

To make a specific property in the layout replace its value in the state file, select the Specific Properties button and add or remove properties. The properties added in the State Wins Over Design list box always replace the feedback values in the layout.

To revert to the default selection, that is the schematic properties will always replace the state file properties, select the Never radio button.

After you have added or removed properties, check if you need to change any other setup options in the other five tabs. To change information in another tab, select the tab and make the required changes. You can click the OK button to accept the changes, or click the Cancel button to ignore the changes.

If you have made any property changes in the current session and want to ignore these changes, click the Reset button.
Note: For more information about the STATE_WINS_OVER_DESIGN and STATE_WINS_OVER_LAYOUT directives, see the Cadence document Packager-XL Reference.

Changing Feedback Properties in the Layout

To change the feedback properties in Packager Setup, select the From Layout tab. See Packager Setup - From Layout Tab on page 46.

Figure 2-5  Packager Setup - From Layout Tab
You can use the *From Layout* tab to make the following changes:

1. Define the feedback properties.
   
   By default, the feedback properties replace the corresponding properties in the schematic. You can, however, specify that certain feedback properties will not replace the properties in the schematic. To specify that a feedback property will not replace the schematic property, add that property in the *No Feedback Properties* list box. To add or remove properties from the *No Feedback Properties* list box, refer to *Adding and Deleting Properties*.

   Click *Remove* in the *No Feedback Properties* list box to delete any property from it. A property removed from the *No Feedback Properties* list box is fed back to the schematic.

   **Note:** The *NO_FEEDBACK* directive is used to prevent feeding back properties to the schematic. For more information about the *NO_FEEDBACK* directive, see the Cadence document *Packager-XL Reference*.

2. Run Packager-XL in the Feedback mode.
   
   By default, the *None* radio button is selected signifying that Packager-XL will run only in the Forward mode.

   To run Packager-XL in the Feedback mode, click either the *Allegro* radio button or the *3rd Party* radio button to specify the source of feedback files.

   If you want feedback from a third party feedback file, select the appropriate feedback file by clicking the check box to its left. You can specify one of the four check boxes:
   
   - *Pstprtx*—Feeds back physical reference designator transformation
   - *Pstnetx*—Feeds back physical net name transformation
   - *Pstsecx*—Feeds back physical reference designator transformation
   - *Pstfnet*—Feeds back connectivity changes for RefDes pin numbers

   **Note:** The *FEEDBACK* directive is used to run Packager-XL in the Feedback mode. For more information about the *FEEDBACK* directive, see the Cadence document *Packager-XL Reference*.

3. Annotate properties.
   
   You can define the objects in the design that must be backannotated. You can select body, pin, net, or physical net name for backannotation. To select any object for backannotation, click the respective check boxes under the *Options* radio button.

   To select all objects, click the *All* radio button.
If you do not want to specify any object for backannotation, select the *None* radio button. The properties that are not backannotated to the schematic are assigned the `ANNOTATE` directive. For more information about the `ANNOTATE` directive, see the Cadence document *Packager-XL Reference*.

4. **Manage hard properties.**

You can manage the packaging of hard properties (user-defined properties) by selecting the *Do not Update Hard Location, Section and Pin numbers on schematic* check box.

By default, Packager-XL updates only soft properties in the Feedback mode. By selecting the *Do not Update Hard Location, Section and Pin numbers on schematic* check box, you can update hard properties.

**Note:** The `HARD_LOC_SEC` directive is used to control the backannotation of hard properties. For more information about the `HARD_LOC_SEC` directive, see the Cadence document *Packager-XL Reference*.

After you have added or removed properties, check if you need to change any other setup options in the other five tabs. To change information in another tab, select the tab and make the required changes. You can click the *OK* button to accept the changes, or click the *Cancel* button to ignore the changes.

If you have made any property changes in the current session and want to ignore these changes, click the *Reset* button.

**Changing Packager Output Information**

To change the output files that Packager-XL generates or to suppress warning messages, select the *Report* tab (See Figure 2-6 on page 49).
You can use the *Report* tab to make the following changes:

1. Define the Packager-XL output files.

   By default, Packager-XL generates the following output files: netlist files (*pstchip.dat*, *pstrxnet.dat*, and *pstrxprt.dat*), a change file (*pxl.chg*), a report file (*pstrpt.dat*), a pinlist file (*pstrpin.dat*), and an Xref file (*pstrxref.dat*). For more information about Packager-XL output files, refer to Forward Mode on page 71.

   If you do not want Packager-XL to generate any output file, select the *None* radio button.
To customize the Packager-XL output files, select the **Custom** radio button and click any of the following check boxes:

- **NetList** check box—Select this check box to generate the netlist files.
- **Change** check box—Select this check box to generate the `pxl.chg` file, which documents the packaging changes between two packager runs.
- **Report** check box—Select this check box to generate the `pstrpt.dat` file, which provides a component summary and spares list.
- **Pinlist** check box—Select this check box to generate the `pstpin.dat` file, which contains a design-specific pin list.
- **Xref** check box - Select this check box to generate the `pstxref.dat` file, which contains information about cross-references between all logical-to-physical assignments, net names, and components.

**Note:** The **OUTPUT** directive specifies the output files generated by Packager-XL. For more information about the **OUTPUT** directive, see the Cadence document *Packager-XL Reference*.

2. **Suppress warnings.**

By default, Packager-XL generates all output warnings and stores them in the `pxl.log` file. You can suppress warnings. To suppress any warning, add the warning number corresponding to that warning in the **Suppress** list box, which is a part of the Add Suppressed Warnings dialog box.

To display the Add Suppressed Warnings dialog box, select the **Add** button in the Packager Setup dialog box. In the Add Suppressed Warnings dialog box, you can suppress any warning by adding its warning number in the **Warning Number** field and clicking **OK**.

**Note:** The **SUPPRESS** directive is used to suppress specific warning messages. For more information about the **SUPPRESS** directive, see the Cadence document *Packager-XL Reference*.

3. **Define the maximum number of errors.**

To change the maximum number of permissible errors that Packager-XL records before terminating an operation, change the number in the **Maximum Errors** field. The default value is **999**.

**Note:** The **MAX_ERRORS** directive is used to specify the maximum numbers of errors allowed before Packager-XL terminates an operation. For more information about the **MAX_ERRORS** directive, see the Cadence document *Packager-XL Reference*. 
4. Define the number of backup versions.

You can use the *Backup Versions* field to define the number of backup (pst) files that Packager-XL will maintain. The default value is three.

**Note:** The `NUM_OLD_VERSIONS` directive is used to define the number of backup (pst) files that Packager-XL will maintain. For more information about the `NUM_OLD_VERSIONS` directive, see the Cadence document *Packager-XL Reference*.

5. Verify that a logical part is assigned to every instance in the design.

You can select the *Check for ppt entry for all instances in design* check box to ensure that ppt entries exist for all instances in the design. If an instance does not have a ppt entry or if the corresponding ptf files are not present, a warning is generated. This warning is recorded in the `pxl.log` file.

After you have added or removed properties, check if you need to change any other setup options in the other five tabs. To change information in another tab, select the tab and make the required changes. You can click the *OK* button to accept the changes, or click the *Cancel* button to ignore the changes.

If you have made any property changes in the current session and want to ignore these changes, click the *Reset* button.

### Changing Reference Designators and Netlist Parameters

![Caution]

*Exercise caution when changing the default-naming scheme for reference designators. To apply a new pattern to the existing reference designators, you must repackage the design.*

To change reference designators and netlist parameters, select the *Layout* tab. See *Packager Setup - Layout Tab* on page 52.
You use the *Layout* tab to make the following changes:

1. Change the reference designator.

   By default, Packager-XL assigns a default reference designator that has two parts, the base name as defined by the `PHYS_DES_PREFIX` property and a number that is appended by Packager-XL. If you need to specify a reference designator that is different from the default, specify its value in the *Ref Des Pattern* field.

   **Note:** The `REF_DES_PATTERN` directive is used to specify the format of reference designators assigned to the physical parts in the design. See the Cadence document *Packager-XL Reference* for more information about the `REF_DES_PATTERN` directive.
If you want to reset the Ref Des counter for new pages and different Ref Des prefixes, then select the *Reset Ref Des counter for new pages and Ref Des prefix* check box.

2. Specify that you want to reuse reference designator numbers.

   By default, the *Reuse Ref Des numbers* check box is selected signifying that Packager-XL can use the reference designators of changed or deleted components in the schematic or the board for new components. If you do not want to reuse existing reference designators, clear the *Reuse Ref Des numbers* check box.

   **Note:** The **REUSE_REFDES** directive is used to control the reuse of reference designators in a project. For more information about the **REUSE_REFDES** directive, see the Cadence document *Packager-XL Reference*.

3. Change the default reference designator prefix.

   By default, Packager-XL uses U as the reference designator prefix. If you have a **PHYS_DES_PREFIX** property that is different from U, type its value in the *Default Ref Des Prefix* field.

4. Change the default reference designator length.

   By default, Packager-XL uses a maximum of 31 characters for defining reference designators. If you want to change the default length, enter a number for the new length in the *Ref Des Length* field.

   **Note:** The **REF_DES_LENGTH** directive is used to control the maximum length of the physical reference designators generated by Packager-XL. For more information about the **REF_DES_LENGTH** directive, see the Cadence document *Packager-XL Reference*.

5. Change the default part type length.

   By default, Packager-XL uses a maximum length of 31 characters for defining component names. If you want to change the default length, enter a number for the new default length in the *Part Type Length* field.

   **Note:** The **PART_TYPE_LENGTH** directive is used to control the maximum length of the synthesized part names generated by Packager-XL. For more information about the **PART_TYPE_LENGTH** directive, see the Cadence document *Packager-XL Reference*.

6. Change the default net name length.

   By default, Packager-XL uses a maximum length of 31 characters for defining net names. If you want to change the default length, enter a number for the new default length in the *Net Name Length* field.

   **Note:** When you change the default value, the new value does not become effective
automatically. You must repackage the design for the new value to become effective.

**Note:** The **NET_NAME_LENGTH** directive is used to control the maximum length of the physical net names generated by Packager-XL. For more information about the **NET_NAME_LENGTH** directive, see the Cadence document *Packager-XL Reference.*

7. Define the list of characters that will be included in net names.

You can change the list of characters that will be included in defining net names. To add a new character, click the *Add* button. This will display the Add Net Characters dialog box where you can add a character. To remove any character, select it in the *Net Characters* list and click *Remove.*

**Note:** The **NET_NAME_CHARS** directive is used to specify special (non-alphanumeric) characters permitted in physical net names. For more information about the **NET_NAME_CHARS** directive, see the Cadence document *Packager-XL Reference.*

After you have added or removed properties, check if you need to change any other setup options in the other five tabs. To change information in another tab, select the tab and make the required changes. You can click the *OK* button to accept the changes, or click the *Cancel* button to ignore the changes.

If you have made any property changes in the current session and want to ignore these changes, click the *Reset* button.

### Changing Setup Options While Packaging Subdesigns

To change the setup options while packaging subdesigns, select the *Subdesign* tab. See *Packager Setup - Subdesign Tab* on page 55.
You use the Subdesign tab to make the following changes:

1. Generate a subdesign state file.

   Subdesigns are pre-packaged blocks containing logic that can be reused in the context of larger designs. Using Packager-XL, you can save packaging assignments for a subdesign in a new file called the subdesign state file.

   To generate the subdesign state file, add the name of the design in the Generate Subdesign list box by using the Add button. When you click the Add button, the Add Subdesign dialog box appears. You can enter the name of the design and click the OK
button to add the name of the design in the *Generate Subdesign* list box. The design names entered in this list box are used to prepare the subdesign state files.

You can remove a subdesign from the *Generate Subdesign* list box. To remove the subdesign, select the design name and click the *Remove* button.

**Note:** The `GEN_SUBDESIGN` directive is used to specify the modules for which you want to generate subdesign state files. For more information about the `GEN_SUBDESIGN` directive, see the Cadence document *Packager-XL Reference*.

2. Force packaging in the subdesign.

To apply the packaging in the subdesign state file to each instance of the subdesign, add the names of the design to the *Force Subdesign* list box.

To add or remove design names from the *Force Subdesign* list box, use the *Add* or *Remove* buttons.

**Note:** The `FORCE_SUBDESIGN` directive is used to apply the packaging in the subdesign state file to each instance of the subdesign. For more information about the `FORCE_SUBDESIGN` directive, see the Cadence document *Packager-XL Reference*.

3. Use subdesigns selectively.

If you want to apply the packaging in the subdesign state file only to the new instances of the subdesign, add the name of the design to the *Use Subdesign* list box. This lets you change the subdesign packaging without affecting existing instances of the subdesign.

To add or remove design names from the *Use Subdesign* list box, use the *Add* or *Remove* buttons.

**Note:** The `USE_SUBDESIGN` directive is used to apply the packaging in the subdesign state file only to the new instances of the subdesign. For more information about the `USE_SUBDESIGN` directive, see the Cadence document *Packager-XL Reference*.

4. Define a different character for renaming reference designators for reuse modules

By default, the underscore (_) letter is used by Packager-XL to define the reference designator for reuse modules. If you want to define a different character for renaming reference designators for reuse modules, type that character in the *Subdesign Suffix Separator* field.

**Note:** The `SD_SUFFIX_SEPARATOR` directive is used to define a different character for renaming reference designators for reuse modules. For more information about the `SD_SUFFIX_SEPARATOR` directive, see the Cadence document *Packager-XL Reference*. 


After you have added or removed properties, check if you need to change any other setup options in the other 5 tabs. To change information in another tab, select that tab and make the required changes. You can click the OK button to accept the changes, or click the Cancel button to ignore the changes.

If you have made any property changes in the current session and want to ignore these changes, click the Reset button.
Allegro-Concept Property Flow

Overview

To synchronize the property changes between the schematic prepared in Concept HDL and the board generated in Allegro, use the Visual Design Differences (VDD) tool. VDD compares the schematic and the board and lists all property differences between them. You can synchronize a schematic and a board by accepting the property differences in the board.

However, resolving the property differences between the schematic and the board might be difficult because VDD displays a large number of property differences. Most of these differences are caused because of the inability of VDD to recognize whether or not the following are true:

1. A property is Concept-only. This property belongs only to the schematic and should not be transferred to the board.
2. A property is Allegro-only. This property belongs only to the board and should not be backannotated to the schematic.
3. A property originated from Concept HDL but was deleted in Allegro.

You can use the Property Flow Setup dialog box to define the properties that will flow between Allegro and Concept HDL.

**Note:** See the Cadence document *PCB Systems Properties Reference* for more information about different properties.

Allegro-Concept Property Flow Use Model

Before you package the design, select all properties that will be transferred between Allegro and Concept HDL by using the Property Flow Setup dialog box.

The Property Flow Setup dialog box provides an easy way to update the pxlBA.txt file. This file contains information about which properties can be transferred from Allegro to Concept HDL.
**Note:** If you are moving from Version 13.6, use the existing `pxlba.txt` file to populate all properties in the Property Flow Setup dialog box. For each property that is selected as transferable from Allegro to Concept HDL, click the *Transfer* check box corresponding to it in the Property Flow Setup dialog box.

## Properties Flow from Allegro to Concept HDL

The properties flow from Allegro to Concept HDL is summarized in the following figure:

**Figure 3-1 Property Flow**

The inputs to the Property Flow Setup dialog box are:

1. The Cadence default `propflow.txt` file—This file defines the default properties that flow between Allegro and Concept HDL.

2. `pxlba.txt` file—The `pxlba.txt` file is used to define the properties that are backannotated to Concept HDL. This file is located in the physical view of the root design.
Note: Property Flow Setup does not automatically pick all properties from the pxlba.txt file. If you have customized the pxlba.txt file from a previous release, then use the information contained in it to populate the Property Flow Setup dialog box.

The Property Flow Setup dialog box accepts the above inputs and allows you to modify the existing properties and add new properties. When you save the changes in the Property Flow Setup dialog box, the pxlba.txt file is updated. This file is used by VDD and Genfeedformat to determine the default properties that flow between Allegro and Concept HDL.

Opening the Property Flow Setup Dialog Box

1. Display the Export Physical dialog box.

To display the Export Physical dialog box,

- Choose Export Physical from the File menu in Concept HDL.
- Click the Design Sync icon in Project Manager, and click the Export Physical option.

The Export Physical dialog box appears.
2. Click the Advanced button.

The Packager Setup dialog box appears.
3. Click the *Property Flow Setup* button.

   The Property Flow Setup dialog box appears.
Figure 3-4  Property Flow Setup Dialog Box

Note: You can also launch the Property Flow Setup dialog box from VDD by choosing the Property Flow Setup option from the Difference menu.

Note: The use of the Property Flow Setup dialog box does not change the front-to-back flow. For more information about the front-to-back flow, see Front-to-back Flow: Traditional Flow on page 19.

Setting the Property Flow

To set the property flow, you need to include and exclude properties in the Property Flow Setup dialog box. By default, the Property Flow Setup dialog box picks the properties from
the propflow.txt file (<your_inst_dir>/share/cdssetup/propflow.txt). These properties are displayed in a grid box with five columns representing the property name, the object to which these properties are attached, information about whether properties are defined in Allegro or Concept HDL, and whether each property will be transferred from Allegro to Concept HDL along with the netlist.

You can change the default properties in one of the following four ways:

1. Add a new property.
2. Delete an existing property.
3. Edit the values for a property.
4. Import properties from another file (pxlba.txt or pst*.dat files).

Adding New Properties

1. Click at the number to the left of the property name after which the new property is to be created.

2. Click the Add button.

   A new property row is created. The Property name is blank. The Owner field is filled based on the object to which the property is attached. The Defined In check boxes are selected for both Concept HDL and Allegro. The Transfer check box is grayed out.

   **Note:** You can define a new name for the property.

3. To change the owner, select the Owner field for the new property.

4. A list button appears. Click the list button and click one of the four options: Comp, Pin, Function, and Net.

   **Note:** If you need to add a property as a Comp property, add the property in the list of properties defined by the COMP_INST_PROP directive.

5. If the new property is not defined in Concept HDL or Allegro, clear the check box corresponding to Concept or Allegro in the Defined In fields.

6. If the property can be transferred from Allegro to Concept HDL along with the netlist, select the Transfer check box.

7. To accept the property changes and close the Property Flow Setup dialog box, click the OK button. To ignore the property changes and close the Property Flow Setup dialog box, click the Cancel button.
Deleting Properties

1. To delete a property, select the property by clicking the number to the left of the property name.
2. Click the Delete button.
3. To accept the property changes and close the Property Flow Setup dialog box, click the OK button. To ignore the property changes and close the Property Flow Setup dialog box, click the Cancel button.

Editing Properties

1. To edit a property name, select the property name by triple-clicking in the Property field and type the new name.
   
   **Note:** Editing a property name is rarely required. Unless you have made a spelling error while defining the property name, avoid editing the property name.

2. To change the owner of the property, select the new option in the Owner field.
3. To set the property as defined in Concept HDL or Allegro, select or clear the check box corresponding to Concept or Allegro in the Defined In fields.
4. To define a property as transferable, select the Defined In Concept and Defined In Allegro property. Next, select the Transfer check box.
5. To accept the property changes and close the Property Flow Setup dialog box, click the OK button. To ignore the property changes and close the Property Flow Setup dialog box, click the Cancel button.

Importing Properties

1. To import properties from the pxlba.txt file or the pst*.dat files, click the Import button.
   
   The Import From dialog box appears. The Px1ba File radio button is selected by default.
2. The `pxlba.txt` file for the project (located in the physical view under the root design) appears selected in the *Pxlba File* field. To change the path of the `pxlba.txt` file, click the browse button and select the new file.

3. To import the properties from the packaged directory, select the *Packaged Directory* radio button. The *Packaged Directory* field displays the path to the packaged directory of the root design. You can change this path by using the browse button.

4. To accept the property changes and close the Property Flow Setup dialog box, click the *OK* button. To ignore the property changes and close the Property Flow Setup dialog box, click the *Cancel* button.

   If you click *OK*, the Import From dialog box closes and a new set of properties is added to the property list in the Property Flow Setup dialog box.

**How properties from the pxlba.txt file are seeded in the Property Flow Setup dialog box**

Packager-XL reads all properties defined in the `pxlba.txt` file. For each property definition that does not exist in the Property Flow Setup dialog box, Packager-XL creates a new row with the following attributes:

- The property name is filled in the *Name* field.
- The owner field shows the owner type specified in the `pxlba.txt` file.
- The *Concept* and *Allegro* check boxes are selected.
- The *Transfer* check box is selected signifying that the property will be transferred from Allegro to Concept HDL.
If the property name already appears in the Property Flow Setup dialog box and the owner type is the same as in the pxlba.txt file, the following check boxes for the property are selected:

- Concept
- Allegro
- Transfer

If the property name already exists in the Property Flow Setup dialog box and the owner type is different from that in the pxlba.txt file, a new row is added to the dialog box with property values same as those for a new property.

How properties from Packager files are seeded in the Property Flow Setup dialog box

All properties defined in the Packager (*pst*.dat) files are read by the Property Flow Setup dialog box. A predefined list of properties that are used by Cadence tools is filtered out. To view the list of properties filtered using the Property Flow Setup dialog box, refer to the List of Properties Filtered from Packager Files. For each property definition that does not exist in the Property Flow Setup dialog box, a new row is created with the following attributes:

- The property name is filled in the Name field.
- The Owner field is filled based on the object to which the property is attached.
  - If the object is attached to a package, the owner defined is a component.
  - If the object is attached to an instance, the owner defined is a function.
  - If the object is attached to a pin, the owner defined is a pin.
  - If the object is attached to a net, the owner defined is a net.
- The Concept check box is selected.
- The Allegro check box is not selected.
- The Transfer check box is grayed out because the Allegro check box is not selected.

If the property name already exists in the Property Flow Setup dialog box and the owner type is the same as for the existing property, the Defined In Concept check box is selected for the row.

If the property name already exists in the Property Flow Setup dialog box and the owner type is different in the *pst*.dat files, the property is considered a new property. A new row is added to the dialog box with the property values being the same as those for the new property.
Packaging Your Design

Overview

Packager-XL is the interface between the schematic and the board for the Cadence Board Design solution.

You can use this tool to

- Translate the schematic into a physical design
- Backannotate the changes made in the board to the schematic
- Update the changes made in the schematic after initial packaging to the board

Note: While the translation is done only once, backannotation and updating can be done multiple times to bring the schematic and the board in sync, that is, they have identical information.

Figure 4-1 Packager-XL and Synchronizing the Schematic and the Board
Where Packager-XL Fits in the PCB Design Process

Packager-XL forms the middle layer of the PCB design process. It acts as a bridge between the design entry phase, which involves preparing the schematic, and the board creation phase, which involves creating the layout.

Figure 4-2  Project Manager with the Board Design Flow

Design Sync Includes
- Export Physical
- Import Physical
- Design Differences
Packager-XL Operation Modes

Packager-XL works in the following two modes:

- **Forward Mode**
  
  In the Forward mode, Packager-XL translates a logical design entered in Concept HDL into a physical design ready for layout in Allegro. To run the Forward mode, you need to run the `Export Physical` command.

- **Feedback Mode**
  
  In the Feedback mode, Packager-XL receives changes made in Allegro and incorporates these changes into the logical design. To run the Feedback mode, you need to run the `Import Physical` command.

Packager-XL uses the standard Hardware Description Language (HDL) naming conventions to simplify intertool communication. The library structure used is based on the Library-Cell-View model and is common across all Cadence solutions.

After packaging a design, Packager-XL places HDL-based netlist files in a packaged view within the design cell view as shown in the `HDL-Based Directory Structure` figure on page 71.
Forward Mode

In the Forward mode, you enter a design in Concept HDL, and then run Packager-XL to translate the logical design into a physical design. This process is also known as packaging the design into physical parts. To incorporate incremental design changes into the existing physical design, you can use subsequent Packager-XL runs. To import the packaged design into the Allegro environment, you use the Allegro Import Logic program.

Depending on whether you are using traditional flow or Constraint Manager enabled flow, Allegro reads 3 or 5 pst*.dat files. In the traditional flow, Allegro reads pstxprt.dat, pstxnet.dat, and pstchip.dat netlist (output) files. In the Constraint Manager enabled flow, Allegro reads pstxprt.dat, pstxnet.dat, pstchip.dat, pstcmdb.dat and pstcmbc.dat files. Based on information contained in these files, Allegro produces or updates an Allegro layout file. See the Forward Mode of Operation figure on page 72 for details.
Note: See Front-to-back Flow: Traditional Flow on page 19 for and Front-to-back: Constraint Manager Enabled Flow on page 22 for more information about the different files used in the two design flows.

Figure 4-4 Forward Mode of Operation

* CM enabled flow includes all files in the traditional flow and some additional files as mentioned in the figure.

 Inputs in the Forward Mode

The inputs to Packager-XL during the Forward mode are as described below:
1. Setup information
   Packager-XL obtains its setup information from the project file (.cpm).

2. Design entered in Concept HDL
   Design saved in Concept HDL generates the `verilog.v`, `viewprps.prp`, and SIR files. The `verilog.v` file contains connectivity information (information about the structure of the design). The `viewprps.prp` file contains information about all properties in the schematic. The SIR file contains information for EDB to create an expanded view of the design.

3. Electrical constraint file
   If you run Constraint Manager from Concept HDL, then it creates `<root_design>.dcf` file, which contains a snapshot of electrical constraint information in the design. This file is available in the constraints view under the root design. If this file is present, Packager-XL reads electrical constraint information from it will get filtered and Packager-XL will run in the Constraint Manager enabled flow.

4. OPF file
   Packager-XL uses the information in the OPF file for occurrence properties as input.

5. Library data
   Packager-XL uses the library chips files and Physical Part Tables (PPTs) to obtain the physical information for the schematic instances used in the design.

6. State file, `pxl.state`
   Packager-XL uses the state file as an input file to maintain the packaged design for subsequent runs of Packager-XL.

**Outputs From the Forward Mode**

The outputs produced by Packager-XL in the Forward mode are as described below:

1. `pxl.state`
   Packager-XL uses the state file to store the packaging assignments for subsequent runs. The `pxl.state` file stores the mapping information for physical nets, differences between the schematic and the layout, and instance-specific information for reused hierarchical or structured blocks.

2. `pxl.log`
Packager-XL dumps any warnings and errors encountered during the Packager-XL run in the pxl.log file. This file also includes the values of directives used and run statistics such as elapsed time.

3. *pstchip.dat*, *pstxprt.dat*, and *pstxnet.dat*

   Packager-XL generates three netlist files, *pstchip.dat*, *pstxprt.dat*, and *pstxnet.dat*. These files are imported by Allegro to create or update a board. Packager-XL utilities, such as the Bill of Materials (BOM), also use netlist files to generate BOM reports.

4. *pstmtdb.dat*, *pstmtbc.dat*

   Packager-XL generates the above 2 files (in addition to all other files mentioned in this section) when it runs in the Constraint Manager enabled flow. These files contain information about the current electrical constraints for the design. If you are running Packager-XL in the traditional flow then information about the current electrical constraints for the design is stored in the *pstxnet.dat* file.

5. *pstback.dat*

   Packager-XL generates the *pstback.dat* file, which backannotates the Concept HDL schematic with packaging information, such as reference designator assignments and physical pin numbers. Backannotation is done using the `backannotate` command in Concept HDL.

6. *pxl.chg*

   Packager-XL dumps the differences in packaging between two consecutive runs of Packager-XL in the *pxl.chg* file. This file contains a list of the binding changes, logical changes, physical changes, and net changes.

7. *pstmtcmb.dat*

   If you are using the Constraint Manager enabled flow, then `Tools > Constraints > Update Schematic` command and `Tools > Back Annotate > Constraint Backannotation` commands create the *pstmtcmb.dat* file. This file contains information about the electrical constraints that require backannotation to the schematic.

   The `Import Logic` program in Allegro uses all Packager-XL output files to import the packaged design.

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**Feedback Mode**

After you have packaged the design and prepared the board, you may add new components, or make property, connectivity, or reference designator changes. These changes cause the
schematic and the board to go “out of sync”. You can use the Feedback mode to incorporate the logical changes and assignments made in the physical layout back to the design. See the Feedback Mode of Operation figure on page 75 for details.

**Figure 4-5 Feedback Mode of Operation**
Inputs to the Feedback Mode

The inputs to Packager-XL during the feedback mode are as described below:

1. Export Logic from Allegro or Import Physical from Packager-XL

   To extract information from the physical layout and create feedback files for Packager-XL, you use the Allegro Export Logic program.

2. pxlba.txt (You can use Property Flow Setup UI to generate this file)

   To change backannotation information, you can modify the pxlba.txt file. This file is used by the Allegro Export Logic program to determine the properties included in the feedback files.

3. Allegro feedback files (pinview.dat, funcview.dat, netview.dat, and compview.dat)

   Allegro feedback files are produced by genfeedformat. These files store the following information:

   - pinview.dat—This file stores information about connectivity and pin instance properties.
   - funcview.dat—This file stores property information for schematic instances.
   - netview.dat—This file stores property information for nets.
   - compview.dat—This file stores property information for component instances.

   Allegro feedback files provide Packager-XL inputs about all changes that are made in the board.

   In the Constraint Manager enabled flow, besides the above 4 *view.dat files, Packager-XL also uses the following 2 files, which are generated by genfeedformat when you run Import Physical or Export Logic from Allegro:

   - cmdbview.dat—This file stores information about the current electrical constraints for the design.
   - cmbcview.dat—This file stores the electrical constraint information for the design used by the board during the last time when it was updated.

4. Third-Party Feedback Files

   If you are running a third-party layout tool, you can produce four feedback files (pstfnet.dat, pstrpx.dat, pstsecx.dat and pstnetx.dat) and use them as input to Packager-XL during the Feedback mode. These files store the following information:
Packaging Your Design

- **fstfnet.dat**—This file describes the connectivity for each reference designator pin number in the design. You require this file as an alternate feedback file from third-party layout systems other than Allegro.

- **stprtx.dat**—This file describes the physical reference designator changes.

- **stsecx.dat**—This file describes section changes. Using this file, you can reassign logical parts within the same physical package or to another physical package.

- **stnetx.dat**—This file describes the physical net name changes.

You use either Allegro feedback files or third-party feedback files but not both.

**Outputs From the Feedback Mode**

After receiving inputs, Packager-XL produces output files, which include the **stback.dat** file used by Concept HDL for backannotation.

Packager-XL produces the following files in the Feedback mode:

1. **stback.dat**—Concept HDL uses this file to backannotate to the base schematic.

2. **pxl.state**—Packager-XL updates the pxl.state file to store packaging information about future runs.

3. **OPF**—Packager-XL updates the OPF file with any change in property or connectivity information that might have occurred in the board after the initial transfer of packaging information from the schematic.

4. Output files—Packager-XL generates the following output files: **stchip.dat, stxprt.dat, stxnet.dat, pxl.log, and pxl.chg.** These output files are updated so that future runs by Allegro get the right packaging information. The output files generated by Packager-XL in the Feedback mode are the same as the output files generated in the Forward mode.

   In the Constraint Manager enabled flow, Packager-XL generates two more pst files, **stcmdb.dat** and **stcmdc.dat**.

**Properties and Directives**

You can use Packager-XL properties to control the packaging of the schematic. You can control the flow of properties between Packager-XL and the layout tool using Packager directives.
Packager Properties

You can assign properties to do the following:

- Define unique physical components or devices by using component definition properties.
- Assign schematic instances to specific reference designators or sections (using the LOCATION property and the SECTION command in Concept HDL).
- Swap pins within sections (using the PINSWAP command in Concept HDL).
- Group schematic instances (using the GROUP property), or assign schematic instances to specific areas on the board (using the ROOM property).
- Mark schematic instances for special handling during packaging (using the PACK_IGNORE and PACK_SHORT properties).

During the packaging of a design, Packager-XL makes packaging assignments for all schematic instances that do not have user-assigned values. These assignments are saved in the state file for use in future runs of Packager-XL. These assignments are also written to the backannotation file pstback.dat, which is used by Concept HDL to backannotate properties to the schematic. Packager-XL assignments are backannotated to the Concept HDL schematic as CDS_LOCATION, CDS_SEC, and CDS_PN properties.

Packager-XL backannotates two sets of properties to the Concept HDL drawing.

- Packager-XL properties (CDS_LOCATION, CDS_SEC, and so on)
- Display properties ($LOCATION and $PN)

You can replace Packager-XL-assigned properties. For example, you can edit the $LOCATION or $PN properties and make them work like the LOCATION or PN properties. Packager-XL does not replace the value for the edited $LOCATION or $PN properties. To change the SEC property, you must use the SECTION command in Concept HDL.

Packager Directives

Packager directives are specified in the Packager Setup form and are stored in the project file. These directives allow you to control the flow of properties between Packager-XL and the layout tool.

- FILTER_PROPERTY—Use the FILTER_PROPERTY directive to specify the properties to be omitted from the output files. You can list any number of properties to be omitted.
- PASS_PROPERTY—Use the PASS_PROPERTY directive to specify the properties that are to be passed to the packager output files.
Packaging Your Design

- **REMOVE_FROM_STATE**—Use the **REMOVE_FROM_STATE** directive to specify the properties to be removed from the state file.

- **STATE_WINS_OVER_DESIGN**—Use the **STATE_WINS_OVER_DESIGN** directive to use the property values in the state file to replace the values in the schematic.

- **STATE_WINS_OVER_LAYOUT**—The **STATE_WINS_OVER_LAYOUT** directive is used only when feedback is allowed. By default, the feedback properties are retained in the state file. Use the **STATE_WINS_OVER_LAYOUT** directive to specify that the property values in the state file replace the values in the feedback properties.

**Prerequisites for Running Packager-XL**

Before you run Packager-XL, you need to

- Specify your design and include Packager-XL-specific properties in Concept HDL.

- Create or modify the setup information for Packager-XL. See Chapter 2, “Setting Up Packager-XL” for more information about Packager Setup.

  **Note:** You can create or modify the setup information for Packager-XL using a text editor or the Setup program. However, it is recommended that you change properties using the Packager Setup dialog box.

**Running Packager-XL in the Forward Mode**

**Updating the Board with the Changes in the Schematic**

After you have specified the setup information, you can run Packager-XL from Project Manager or from an operating system prompt.

**Note:** It is not recommended that you run Packager-XL from an operating system prompt.

To run Packager-XL from Project Manager and transfer the logic from the Concept HDL schematic to the Allegro board, do the following steps:

1. Choose the **Design Sync** icon from the Project Manager window and click **Export Physical**.

   **Note:** You can also choose **Tools - Design Sync - Export Physical** to display the Export Physical dialog box.
Depending on whether you are using Constraint Manager to edit electrical constraints in Concept HDL (which means depending on the presence of the `<root_drawing>.dcf` file in the constraints view), Export Physical runs in 2 flows, traditional and Constraint Manager enabled. The Export Physical Dialog Box: Traditional Flow figure on page 80 shows the Export Physical dialog box that appears when Constraint Manager is not used to edit electrical constraints in Concept HDL.

**Figure 4-6 Export Physical Dialog Box: Traditional Flow**

![Export Physical Dialog Box: Traditional Flow](image)

The Export Physical Dialog Box: Constraint Manager Enabled Flow figure on page 81 shows the Export Physical dialog box that appears when Constraint Manager is used to edit electrical constraints in Concept HDL.
2. To package your design before updating the layout data, select the Package Design check box. You have the following options in packaging:

- **Preserve**—Packager-XL uses Preserve as the default packaging option. When the Preserve option is selected, Packager-XL incrementally packages the design. All previous packaging is preserved and only the changes from the last packaging run are added.

- **Optimize**—Packager-XL uses Optimize to package the schematic data into a compact physical design.

- **Repackage**—Packager-XL uses Repackage to ignore all previous packaging results and repackage the design.
3. If you want to regenerate physical net names, select the *Regenerate Physical Net Names* check box.

**Note:** Selecting *Regenerate Physical Net Names* check box is useful if:

- you have changed the net length and you have not selected repackage as the packaging option.
- you are migrating from PSD 13.6 to PSD 14.0 or PSD 14.2.

4. Select a package design setting.

5. If you want to change the Packager-XL setup options, click the *Advanced* button.


6. To update the Allegro board, select the *Update Allegro Board (Netrev)* check box in the Export Physical dialog box.

7. Specify the input and output board files. Enter the name of the existing Allegro file that needs to be updated in the *Input Board File* field. Enter the name of the resulting updated file in the *Output Board File* field. To specify the *Input Board File*, click the *Browse...* button. Packager-XL displays the board files (if any) in the physical sub-directory under the design directory. You can select the board file and click *OK*.

   If you specify the output board file as the same as the input board file, Packager-XL overwrites the existing file. If you specify the output board file as a new file (<any_name>.brd), a new board file is created.

   **Note:** Before you transfer the logic data from Concept HDL, you must create the design database (.brd) file in Allegro. You can create an empty .brd file, or start setting up your design by creating a board outline and defining the layers for the design.

8. To make Allegro rip up an etch from a removed pin to the closes T connection or pin, select the *Allow Etch Removal During ECO* check box.

9. Select the option for placing changed components in layout from those made available by packager-XL. Select one of the following 3 options:

   - **Always**

     This is the default selection. If you load a new design logic into the Allegro or SPECCTRAQuest layout, Allegro automatically replaces all components in the layout with the new components from Packager-XL according to their reference designators.

   - **If same**
Allegro automatically replaces all components in the layout with the new components from Packager-XL but only if the replacement component matches the package symbol, value, and the tolerance of the component in the layout.

- Never

Allegro will never replace any components in the layout with new components. You must make the changes interactively.

10. In the traditional flow, the *Electrical Constraints* options are disabled. You cannot make any selection. However, in the Constraint Manager enabled flow, the *Enable Exports* check box is selected by default. You need to select one of the following two options for exporting constraints from the schematic to the board:

- Overwrite current constraints

Netrev deletes all existing electrical constraint information in the *Output Board File* and replaces it with the electrical constraint information currently available in the schematic.

- Export changes only

Netrev exports only the electrical constraint information that has changed in the schematic since the last export, and updates such constraints in the *Output Board File*.

11. Select the *Backannotate Schematic* check box if you want to backannotate the latest packaged and constraints information to the schematic.

12. In the Export Physical dialog box, click *OK*.

The Progress window appears. Information in the Progress window will change based on the options you selected.
In the traditional flow, the following four steps are performed by Packager-XL:

1. Netlisting the design (Select the Package Design check box)
2. Packaging the design (Select the Package Design check box)
3. Updating the board (Select the Update Allegro Board check box)
4. Backannotating the design (Select the Backannotate Schematic check box)

In the Constraint Manager enabled flow, the following two steps are performed by Packager-XL in addition to the four steps performed in the traditional flow:

1. Extracting schematic constraints (Select the Package Design check box)
2. Generating backannotation files (Select the Backannotate Schematic check box)

When Packager-XL completes packaging the design, it displays a message stating that packaging is completed and whether you want to view the results. If you want to view the results, select the View Results button. The View Files dialog box appears. You can select a file and view it in the default text editor.
Mismatch in View Files Generated Across Different Release/Flows

If you have a Version 14.0 Constraint Manager enabled design and bring it to Version 14.2 by running only genfeedformat, then the pstxnet.dat and pstcmdb.dat files will not have the same tag that is used to identify the flow. Export Physical in such case will generate the following message:

Design Flow is Constraint Manager enabled, pstxnet.dat and pstcmdb.dat do not appear to be from the same feedback step. You will not be able to package the design.

Export Physical will not package the design. However, it will call genfeedformat and generate the *view.dat and pstcmdb.dat files. You can then again package the design.

Errors in Electrical Constraints Extraction

If you have defined an electrical constraint with an incorrect syntax, then you will get the following message:

Figure 4-9 Design Sync Error Message

If you click Yes, the concept2cm.log file opens. It lists the errors. You can fix the error and then run Tools-Constraints-Update Schematic command to update the schematic with proper values.

Using the State File for Successive Packager-XL Runs

After the initial packaging, you can make changes to your design. These changes can include adding and deleting pages, schematic instances, nets, connectivity, and properties. The next time you package the design, Packager-XL does the following:

1. Reads the state file that contains the packaging data from the previous run.

2. Copies the state file information to the relevant parts of your design (parts that have not changed since the previous Packager-XL run). The STATE_WINS_OVER_DESIGN and
REMOVE_FROM_STATE directives control how the state file data is copied to the design. See the Cadence document Packager-XL Reference for more information on how you can use the STATE_WINS_OVER_DESIGN directive.

3. Packages the entire design - Conflicts occur when the state file packaging assignments are in conflict with the assignments you make. For example, if you have modified your schematic by assigning a section to a part that was previously packaged, the assignment in the state file is ignored.

In case of a conflict, Packager-XL reassigns the LOCATION, SEC, and PN properties that it copied from the state file. However, the state file packaging information is preserved whenever possible.

Running Packager-XL in the Feedback Mode

Overview

The following types of changes are made in Allegro:

- Renaming reference designators
- Swapping sections
- Swapping pins
- Updating property values

These changes need to be updated in the schematic. You can run Packager-XL in the Feedback mode to update the changes made in the board back to the schematic.

Updating the Schematic with the Changes in the Board

You need to integrate the layout changes with the existing logical design by running Packager-XL in the Feedback mode.

You can use the following two steps to run Packager-XL in the Feedback mode:

1. Generate the layout feedback files from Allegro or third-party tool.
2. Integrate the layout changes with the existing logical design by running Packager-XL in the Feedback mode.
Using Export Logic to Extract Feedback Files

1. From the Allegro Export Logic function,


   The Export Logic dialog box appears. Depending on whether you are using
   Constraint Manager to edit electrical constraints in Concept HDL (which means
   depending on the presence of the <root_drawing>.dcf file in the constraints
   view), Export Logic runs in 2 flows, traditional and Constraint Manager enabled. The
   Export Logic Dialog Box: Traditional Flow figure on page 87 appears when Export
   Logic detects that the design is in the traditional flow, that is Constraint Manager has
   not been used to edit electrical constraints in Concept HDL.

Figure 4-10  Export Logic Dialog Box: Traditional Flow

![Export Logic Dialog Box: Traditional Flow](image)

The Export Logic Dialog Box: Constraint Manager Enabled Flow figure on page 88
appears when Export Logic detects that the design is in the Constraint Manager
enabled flow, that is Constraint Manager has not been used to edit electrical constraints in Concept HDL.

**Figure 4-11** Export Logic Dialog Box: Constraint Manager Enabled Flow

![Export Logic Dialog Box: Constraint Manager Enabled Flow](image)

**b.** To switch to Constraint Manager enabled flow from the traditional flow, select the *Export using Constraint Manager enabled flow* check box.

**Note:** If you switch to the Constraint Manager enabled flow, you cannot return to the traditional flow. A message box appears stating this fact, if you want to change flow to Constraint Manager enabled, click *Yes.*
Figure 4-12 Export Logic Dialog Box: Traditional Flow

- Select the logic type as **HDL-Concept**.
- Specify the path of the directory where you want to store the exported files.
- Click the *Export Cadence* button.

The 5 feedback (*.view.dat) files are generated.

**Note:** If you run Import Physical and select the *Generate Feedback Files* option, you need not run Export Logic in Allegro.

### Moving From 3 to 6 File Flow: Handling Special Case

If you are in the traditional flow in the Forward mode, 3 pst*.dat file would be generated. Now if in Allegro you run *File - Export - Logic* and select the *Export using Constraint Manager enabled flow* check box, Allegro switches to 6 files-based Constraint Manager enabled flow:

Since the Allegro board was branded as working in traditional flow, do an explicit save of the Allegro board file. This will ensure that the board file is branded as working in the Constraint Manager enabled flow.

Next, run Import Physical and select the *Package Design* check box to package the design. This step will ensure that both Concept HDL and Allegro are running in the Constraint Manager enabled flow.

**Note:** If you do not run Import Physical and run Export Physical immediately after switching to Constraint Manager enabled flow in Allegro, then Netrev will generate an error stating that *pstmdb.dat* and *pstmmbc.dat* files are not found.

### Using Import Physical to Update the Schematic and the Board

You can use the Import Physical dialog box to update the schematic with the changes in the board. To update the schematic with changes in the board using Import Physical, do the following:

Import Physical can run in two flows, traditional and Constraint Manager enabled. If Constraint Manager has not been used to edit electrical constraints in Concept HDL, Import physical runs in the traditional flow otherwise it runs in the Constraint Manager enabled flow. You can move from the traditional flow to the Constraint Manager enabled flow but not vice versa.

The Import Physical Dialog Box: Traditional Flow figure on page 91 appears when Import Physical detects that the design is in the traditional flow. A design is in the traditional flow when:

- No <root_drawing>.dcf file is found in the constraints view.
- The Generate Feedback Files check box is not selected and only 4 pst*.dat files exist in the packaged view.
- The Generate Feedback Files check box is selected but the Extract Constraints check box is not selected.
The Import Physical Dialog Box: Constraint Manager Enabled Flow figure on page 92 appears when Import Physical detects that the design is in the Constraint Manager enabled flow. A design is in the traditional flow when:

- The `<root_drawing>.dcf` file is found in the constraints view.
- 6 `pst*.dat` files exist in the packaged view.
- The Generate Feedback Files check box is selected and the Extract Constraints check box is also selected.
2. Select the *Generate Feedback Files* check box.

**Tip**

You can also use *File > Export > Logic* in Allegro to generate feedback files.

3. Specify the Allegro board name in the *Allegro Board File* field.

4. To integrate the layout changes with the existing logical design, run Packager-XL in the Feedback mode by clicking the *Package Design (Feedback)* check box and selecting the feedback source. You can select either Allegro or 3rd party files for feedback. If you have 3rd party files for feedback, select the feedback files to be generated by selecting the appropriate check boxes.

5. Select the option for exporting constraints from the schematic to the board. These options are available based on whether you are in the Constraint Manager enabled flow or the traditional flow.

- *Extract Constraints* check box
In the Constraint Manager enabled flow, the Extract Constraints check box is selected and grayed. You cannot change it. In the traditional flow, you can select this check box. When you are in the traditional flow and you select the Extract Constraints check box, Import Physical displays the following message:

**Figure 4-15 Import Physical: Warning Message**

![Warning Message](image)

If you select the Yes button, then Import Physical will move to the Constraint Manager enabled flow where electrical constraint information is generated in the cmdbview.dat and the cmbcview.dat files. You cannot switch back to the traditional flow. Therefore if you want to stick to the traditional flow and maintain electrical constraint information in the pstxnet.dat file, click on the No button.

- Overwrite current constraints
  Packager-XL overwrites all existing electrical constraint information in the schematic with the electrical constraint information currently available in the Allegro Board File.

- Import changes only
  Packager-XL will import only the electrical constraint information that has changed in the Allegro Board File since the last import and overwrite such constraints in the schematic.

6. Select the Backannotate Schematic check box if you want all the changes (including changes in constraints) in the board to be backannotated to the schematic when you run Import Physical.

Clear this check box if you do not want the schematic to be backannotated when you run Import Physical. You can perform backannotation later by choosing Tools - Back Annotate in Concept HDL.

**Caution**

*Do not run backannotation if any other user who has write permissions is working on the design. Running backannotation when another user is working on the design results in incomplete backannotation.*
7. Click OK.

The Progress dialog box appears, displaying the progress of the Import Physical process. The feedback files are created from the Allegro or SPECCTRAQuest board. Packager-XL is run in the feedback mode using the feedback files from Allegro. The files used for backannotating the constraint changes in the board to the schematic are created in the packaged view of the root design. The constraints in the board are extracted to a file called `pstcmback.dat`. This file is used to backannotate the changes in constraints in the board to the schematic.

The constraints in the schematic are synchronized with the constraints in the board. If you now start Constraint Manager from Concept HDL, all the electrical constraints that you captured in Allegro/APD or SPECCTRAQuest will appear in Constraint Manager.

Mismatch in View Files Generated Across Different Release/Flows

If the `netview.dat` and `cmdbview.dat` files have not been generated at the same time or they have been hand-edited, then Import Physical generates the following message:

**Figure 4-16 Import Physical: Warning Message**

![Design Sync dialog](image)

Import Physical will not feedback the design. However, it will call `genfeedformat` and generate the `netview.dat` and `cmdbview.dat` files. You can then again feedback the design.

Using the `pxlba.txt` File for Controlling the Backannotation of Properties

**Overview**

The `pxlba.txt` file is a file used during backannotation. It lists the properties that you may need to extract from the Allegro or SPECCTRAQuest layout. Before you run the `Import Physical` command or the `Export Logic` program, you can modify the `pxlba.txt` file to control the properties that you want to extract from the Allegro or SPECCTRAQuest layout. You can extract either standard Allegro properties or Allegro user-defined properties.

The `pxlba.txt` file is located at the following path:
<your_install_dir>/share/pcb/text/views

You can specify the properties in the pxlba.txt file by using the Property Flow Setup button in the Packager Setup - Properties Tab.

Displaying the pxlba.txt File

Note: You can launch the pxlba.txt file from Project Manager, the Packager Setup dialog box, or the Design Differences tool.

Displaying the pxlba.txt file from Project Manager

1. Choose Tools - Packager Utilities - View Results... from the Project Manager menu bar.
2. Click the Physical option.
   The view files in the physical view directory appear in the View Results window.
3. Select the pxlba.txt file from the view files listed.
4. Click OK.

The pxlba.txt file appears in a text editor. You can view or edit this file for properties that you want to be backannotated from the layout during feedback.

Displaying the pxlba.txt File from the Packager Setup Dialog Box

1. Select the Property tab to display the Packager Setup - Properties page of the Packager Setup dialog box.
2. Click the Property Flow Setup button.

The Property Flow Setup dialog box appears. The dialog box provides a graphical interface for changing the properties in the pxlba.txt file.

Displaying the pxlba.txt file from Design Differences

Choose Difference - Property Flow Setup.

The Properties Flow Setup dialog box appears with the default pxlba.txt file loaded. See the Property Flow Setup Dialog Box figure on page 96.
Figure 4-17 Property Flow Setup Dialog Box

The Property Flow Setup dialog box lists the properties that flow between Concept HDL and Allegro. Each property name follows with the property owner name (net, pin, component, or function). You can specify whether the property applies to Concept HDL or to Allegro, or to both Concept HDL and Allegro. If a property applies to both Concept HDL and Allegro, you can specify whether or not the property should be transferred between Concept HDL and Allegro.

For more information about how properties flow between Concept HDL and Allegro, see Allegro-Concept Property Flow on page 58.
Packager-XL Exit Status

After packaging the design, Packager-XL exits displaying one of the following exit status values:

Exit status 0

Message - Packager-XL execution done.

Description - Packager-XL has successfully packaged the design. It did not encounter any errors.

Exit status 1

Message - ERROR Packager-XL exiting with status 1.

Description - Packager-XL has encountered non-fatal errors during the packaging of the design. Packager-XL has generated the netlist files. However, some instances might not have been packaged. You can check the pxl.log file to find the details of the errors encountered.

Exit status 2

Message - FATAL ERROR Packager-XL exiting with status 2.

Description - Packager-XL execution failed. Netlist files are generated.

Exit status 202


Description - Packager-XL has successfully completed executing. ECO (Engineering Change Order) was detected during the feedback. You should synchronize the schematic and the board.

Using Packager Utilities

Overview

Packager utilities are used to
To launch any Packager utility perform the following step:

➤ Choose Tools - Packager Utilities in the Project Manager window and click the appropriate tool.

**Generating the Bill of Materials**

You can use the BOM-HDL tool to generate BOM reports. To generate BOM reports, do the following:

➤ Choose Tools - Packager Utilities - Bill of Materials in Project Manager.

The BOM-HDL dialog box appears.
Figure 4-18 BOM-HDL Dialog Box

1. To change the path to the BOM template file, enter the new path of the template file in the Template File field. Alternatively, you can browse to the new path.

   You can customize the BOM template by clicking the Customize button. See BOM-HDL Help for information on how to customize the BOM template, and use callouts or filters.

2. By default, the BOM report is created in the file named BOM.rpt. To change the path to the output file, enter the new path of the output file in the Output File field. Alternatively, you can browse to the new path.

3. The default BOM report is created in the text format. To change the report format to spreadsheet or HTML, select the respective radio button. If you select the Spreadsheet Format radio button, you can change the delimiter by selecting a new delimiter in the Delimiter field. You can change the delimiter to semicolon, colon, space, dot, or hash.

4. If you have created variants for the design using the Variant Editor tool, you can click the Variant BOM button and select the variant.

   Note: See the Variant Editor Help for more information on creating variants and generating BOM reports for those variants.
Running Electrical Rule Checks

You can use the Electrical Rule Checks dialog box to run electrical rule checks. Using these checks, you can verify whether or not the following conditions are correct:

- All outputs on a net have the same output type.
- All nets have at least two nodes (pins) attached to them.
- Each net has at least one input pin and output pin. If there is a bi-directional net, then it must have two pins.
- Each output pin on the net has sufficient drive for the input loading on the net.
- Each pin in the design is defined as input, output, or bi-directional.

**Note:** Before running Electrical Rule Checks, you must have packaged your design to obtain the required netlist files: `pstchip.dat`, `pstxprt.dat`, and `pstxnet.dat`.

To display the Electrical Rule Check dialog box,

➤ Choose *Tools - Packager Utilities - Electrical Rules* in Project Manager.

The Electrical Rule Checks dialog box appears.

Figure 4-19 Electrical Rules Check Dialog Box

To perform electrical rule checks, do the following:

1. To check that all outputs on a net have the same output type, select the *Compatible Outputs* check box.
2. To check that every net has at least two nodes (pins) attached to it, select the *Single Node Nets* check box.

3. To check that each net has at least one input pin and one output pin, select the *Source/Driver* check box.

   **Note:** To override the source/driver check for a pin or a net, attach the *NO_IO_CHECK* property to it. You can also suppress the error by not selecting the *Source/Driver* check box.

4. To check that each output pin on the net has sufficient drive for input loading on the net, select the *Net Loading* check box.

   **Note:** To override the net loading check for a pin or a net, attach the *NO_LOAD_CHECK* or the *UNKNOWN_LOADING* property to it. You can also suppress the error by not selecting the *Net Loading* check box.

5. To check that each pin in the design is defined as input, output, or bi-directional, select the *Pin Direction* check box.

   **Note:** To override the pin direction check for a pin or a net, attach the *NO_DIR_CHECK* property to it. You can also suppress the error by not selecting the *Pin Direction* check box.

6. To perform electrical rule checks, click the *Run* button.

A new report file, *erc.rpt*, containing a summary of violations, severity levels, and directive settings is produced. You can select the *View* button to open the *erc.rpt* file and view it.

**Generating Netlist Reports**

You can use the Netlist Reports dialog box to view or generate netlist reports. You can also select the format in which you would like a report to appear.

**Note:** Before generating netlist reports, you must have packaged your design to obtain the required netlist files: *pstchip.dat*, *pstxprt.dat*, and *pстxnet.dat*.

To generate a netlist report:

1. Launch the Netlist Reports dialog box by using one of the following methods:

   - Choose *Tools - Packager Utilities - Netlist Reports* in Project Manager.
   - Choose *Tools - Packager Utilities - Netlist Reports* in the Concept HDL schematic editor.

   The Netlist Reports dialog box appears. See *Netlist Reports Dialog Box* on page 102.
2. To list the nets in the design that have a minimum of two nodes, select the Concise Netlist (diacnet.dat) radio button. The diacnet.dat file stores the concise netlist. This file is ordered by nets.

3. To list the nets in the design that have a minimum of two nodes that are ordered by physical part designator (body) information, select the Concise Body-Ordered Netlist (dialbonl.dat) check box.

4. To list the part types used in the design and their quantities, select the Concise Parts List (dialcprt.dat) check box.

5. To list the physical part designators for each part type used in the design and their power and ground pins, select the Power and Ground List (dialpgnd.dat) check box.

6. To list the part types used in the design and their reference designators, select the Power and Ground List (dialstf.dat) check box.

7. To generate the selected reports, click the Run button.

8. To view the current version of any report file you selected (for example, the Concise netlist diacnet.dat file), click the View button.

9. To close the Netlist Reports dialog box, click the Close button.
Viewing Any File

You can view any file in the packaged view (created by Packager-XL) or the physical view (created by Allegro or SPECCTRAQuest) by using the View Results dialog box.

To view any file,


   The View Results dialog box appears.

2. Select the Packaged or Physical radio button based on whether you want to see the view files from the packaged view directory or from the physical view directory. The default option is Packaged.

3. Highlight the file that you need to view from this list (for example, *view.dat, *.mkr, *.log, and so on from the packed view or *.log, *.brd, *.jrl, and so on from the physical view) and click OK.

   The selected file is displayed in a text editor. You can use the text editor to edit or print the file.

4. To close the View Results dialog box without viewing any file, click the Cancel button.
Resolving Design Differences

Overview

The development of any design involves an iterative process of synchronizing the differences between the schematic and the board. Changes especially caused by Engineering Change Orders (ECOs) are made in the schematic and need to be updated in the board. Similarly, changes in the board such as reference designator changes and section and pin swaps require updating the board.

You can use the Design Differences tool (also called Visual Design Differences or VDD) to compare the Logical View (that is the packaged representation of the design) and the Physical View (that is the connectivity representation of the layout design) and list the differences. The differences listed by the Design Differences tool includes the following:

- Net, instance, instance part (reference designator), and pin connectivity differences
- Property differences for instances, nets, or pins
- Swapping differences for functions, pins, or reference designators

You can use the Design Differences tool to synchronize any of the above differences.

How the Design Differences Tool Fits in the Front-to-Back Flow

The Design Differences tool fits in the middle of the front-to-back flow. It uses the files produced by Packager-XL in the Forward mode (the PXL files) and the feedback files generated by Genfeedformat to obtain the property and connectivity differences between the schematic and the board. Design Differences updates the property changes in the board back to the schematic. Design Differences also generate the dessync.mkr file, which lists the connectivity differences between the schematic and the board. This file is used by Design Association to backannotate the connectivity differences to the schematic. For more details, see Design Differences: Traditional Flow on page 105.
Figure 5-1  Design Differences: Traditional Flow

Start here

Concept HDL

Property changes / backannotation

Schematic

Packager-XL (Export Physical)

PXL files (3 pst*.dat files)

Netrev

Design Association

Dessync.mkr

PXL files (*view.dat)

Design Differences

Packager-XL (Import Physical)

Feedback files
(4 *view.dat files)

Genfeedformat

Board files

Backward flow

Allegro or SPECCTRAQuest

Inputs for Design Differences

Forward Flow

Backannotate changes

Connectivity changes

Front End

Front-to-Back

Back End
You can make changes in Allegro and then feed back the property changes to the schematic by generating the feedback files using genfeedformat.

You can then use the VDD tool to update the property changes either to the board or to the schematic. When you run VDD, it displays differences in properties between the schematic and the board in multiple windows. See Differences View Windows: Traditional Flow on page 114 for more information about difference windows.

To update the connectivity changes made in the board to the schematic, use the DA tool. DA uses a file generated by VDD named dessync.mkr (which captures connectivity information) to guide you in updating the schematic.

**Note:** While the Design Synchronization toolset helps you synchronize logical-to-physical design differences, it does not allow you to synchronize logical-to-logical or physical-to-physical differences. This implies that you cannot synchronize two schematics or two boards with the Design Synchronization toolset.

You can use the Property Flow Setup dialog box to define the properties that should be transferred between the board and the schematic. The improved property flow allows Design Differences to have a smoother run as it has to capture fewer property mismatches.

**Design Synchronization Flow: Constraint Manager Enabled Flow**

The primary difference between design synchronization flow in the traditional flow and the Constraint Manager enabled flow is the use of Constraint Manager for managing electrical constraints. If you use Constraint Manager in Concept HDL to manage electrical constraints, then Constraint Manager dumps information about electrical constraints in a new view named constraints under the root design. This view includes a file named `<root_design>.dcf`, which contains a snapshot of electrical constraint information in the design.
Figure 5-2  Design Differences: Constraint Manager Enabled Flow

1. Start here
   - Concept HDL
   - Constraint Manager
   - Design Association
   - Packager-XL (Export Physical)
   - Schematic
   - PXL files (5 pst*.dat files)
   - PXL feedback

2. Netrev
   - PXL files
   - Dessync.mkr
   - Feedback files (6 *view.dat files)
   - Design Differences

3. Allegro or SPECCTRAQuest
   - Board files
   - Backward flow
   - Front End
   - Front-to-Back
   - Back End

Forward Flow

Inputs for Design Differences

Backannotate changes

Connectivity changes

Property changes / backannotation

Design Association

Genfeedformat

Packager-XL (Import Physical)
Design Differences Functions

The Design Differences tool does the following:

- Generates differences between the logical and physical views and lists them
- Filters specific differences so that you can view differences of specific interest
- Displays the objects in the entire logical and physical design as a hierarchical tree composed of components, nets, and parts
- Generates the dessync.mkr file, which captures connectivity change information and is used by the Design Association tool to backannotate physical connectivity changes to the Concept HDL schematic
- Queries on a design by part name, reference designator, net name, and property name-value pairs
- Cross-probes instances, nets, and pins on a Concept HDL schematic design, or an Allegro board, or a SPECCTRAQuest layout design to display the source of the differences
- Synchronizes either the logical design or the physical design based on where you want to accept the individual differences

Running Design Differences

To run Design Differences, complete the following steps:

1. The first step in opening the Design Differences tool is to load the Design Differences dialog box. You can load the Design Differences dialog box using one of the following three methods:
   b. Choose the Design Sync icon in Project Manager and select Design Differences.

The Design Differences command finds differences between the board (physical data in the Allegro or SPECCTRAQuest layout) and the schematic (logical data in the Concept HDL schematic) when they are “out of sync”. To run the Design Differences command, you use the Design Differences dialog box. Design Differences may run in 2 modes, Non-CM and CM.
Traditional flow: This is the default flow. In this flow, Design Differences does not distinguish electrical properties differences from other properties and displays the differences between the schematic and the board in the net and properties difference windows.

The traditional flow is selected when `<root_drawing>.dcf` file is not found in the constraints view and none of the `pстcmdb.dat` or `cmbcview.dat` or `cmdbview.dat` files are present in the packaged view.

The Figure 5-3 on page 109 displays Design Differences dialog box in the traditional flow.

Constraint Manager enabled flow: In the Constraint Manager enabled flow, Design Differences displays constraint differences in 2 new Constraints Differences windows, one each for logical and physical domain. Any constraint property differences are filtered from the net-properties difference windows and displayed in the new windows.

The Constraint Manager enabled flow is selected when `<root_drawing>.dcf` file is found in the constraints view or the `pстcmdb.dat` or `cmbcview.dat` or `cmdbview.dat` files are present in the packaged view.

The Figure 5-4 on page 110 displays the Design Differences dialog box in the Constraint Manager enabled flow.
2. The *Update board view before compare* check box is deselected by default. To reextract the physical view from the layout before generating the design differences, select this check box. If the *Update board view before compare* check box is selected, the default board name appears in the *Allegro Board* field.

3. To select a different board than the default, select *Browse* next to the *Allegro Board* field and browse to the file.

4. To switch to the Constraint Manager enabled flow from the traditional flow, select the *Extract Constraints* check box. When you select the *Extract Constraints* check box, Design Differences filters constraint property differences from the net-properties difference windows and displays them in the Constraints Differences windows.

5. The *Update package view before compare* check box is deselected by default. To repackage the logical view from the schematic before generating the design differences, select this check box. If the *Update package view before compare* check box is selected, the default packaged view appears in the *Package View* field.

6. To select a different view than the default, select *Browse* next to the *Package View* field and browse to the file.

7. To compare the differences, click *OK*.

   The Progress window appears.

   When you run Design Differences with the Update package view before compare check box as selected, Design Differences calls Export Physical in a special mode (see Export Physical: Design Differences Mode figure on page 111) where the Update Allegro Board
option is grayed. You can then package and/or backannotate the design. Based on your selection, Export Physical will run. When Export Physical has completed its operation, control is passed back to the Design Differences progress window. Design Differences will complete its progress and display difference windows.

Figure 5-5 Export Physical: Design Differences Mode

![Export Physical - atm.cpm](image)

8. Click OK.

After Export Physical completes its operation, it passes the control back to the Design Differences tool. The Design Differences window appears displaying multiple difference view windows based on the property and connectivity differences in the design.
Design Differences User Interface

The Design Differences tool supports a simple, intuitive graphical user interface for displaying differences between the schematic and the layout. This user interface consists primarily of a menu bar, a toolbar, and multiple design differences view windows.

Design Differences Toolbar

The Design Differences window includes a toolbar with 18 tool buttons. These toolbar icons provide quick access to Design Differences functions.

The figure below displays the Design Differences toolbar.

Figure 5-6  Design Differences Toolbar

![Design Differences Toolbar](image)

The toolbuttons that are grayed out, such as the toolbutton corresponding to the number 13, are inactive. If you place the pointer over a toolbutton, a descriptive label will appear.

The table below describes the function of each toolbutton.

Table 5-1  Design Differences Toolbar: Description

<table>
<thead>
<tr>
<th>S No.</th>
<th>Label</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Instance Difference</td>
<td>Executes the Difference - Instance command and displays the Instance Difference window.</td>
</tr>
<tr>
<td>2</td>
<td>Instance Part Difference</td>
<td>Executes the Difference - Instance Part command and displays the Instance Part Difference window.</td>
</tr>
<tr>
<td>3</td>
<td>Net Difference</td>
<td>Executes the Difference - Net command and displays the Net Difference window.</td>
</tr>
<tr>
<td>4</td>
<td>Pin Connection Difference</td>
<td>Executes the Difference - Pin Connection command and displays the Pin-Net Connection Difference window.</td>
</tr>
</tbody>
</table>
## Resolving Design Differences

<table>
<thead>
<tr>
<th>S No.</th>
<th>Label</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>Property Difference</td>
<td>Executes the Difference - Instance Property command and displays the Instance Property Difference window.</td>
</tr>
<tr>
<td>6</td>
<td>Pin Swap</td>
<td>Executes the Difference - Pin Swap command and displays the Pin-Swapping Difference window.</td>
</tr>
<tr>
<td>7</td>
<td>Section Swap</td>
<td>Executes the Difference - Section Swap command and displays the Section-Swapping Difference window.</td>
</tr>
<tr>
<td>8</td>
<td>RefDes Rename</td>
<td>Executes the Difference - RefDes Rename command and displays the RefDes Difference window.</td>
</tr>
<tr>
<td>9</td>
<td>Filter Options</td>
<td>Executes the Difference - Filter Options dialog box and displays the Filter Options for Difference dialog box.</td>
</tr>
<tr>
<td>10</td>
<td>Update Differences</td>
<td>Executes the File - Update Differences command and displays the updated difference view windows when differences exist between the schematic and the layout.</td>
</tr>
<tr>
<td>11</td>
<td>Update Board</td>
<td>Executes the Sync - Update Allegro Board command and displays the Preview ECO on Allegro Board dialog box.</td>
</tr>
<tr>
<td>12</td>
<td>Update Schematic</td>
<td>Executes the Sync - Update Concept Schematic command and displays the Preview ECO on Schematic dialog box.</td>
</tr>
<tr>
<td>13</td>
<td>Stop</td>
<td>Executes the File - Stop Loading command and stops reloading the Concept HDL schematic design or the Allegro or SPECCTRAQuest board layout.</td>
</tr>
<tr>
<td>14</td>
<td>Highlight</td>
<td>Executes the Display - Highlight Source command and highlights the element causing the difference in the schematic and the board.</td>
</tr>
<tr>
<td>15</td>
<td>Dehighlight</td>
<td>Executes the Display - Dehighlight Source command and removes the highlight from the element causing the difference in the schematic and the board.</td>
</tr>
<tr>
<td>16</td>
<td>Explore (Logical) Design</td>
<td>Executes the Explore - Logical Design command and displays the Logical Design View window.</td>
</tr>
</tbody>
</table>
Design Differences Windows

Differences View Windows: Traditional Flow

Design Differences displays the difference between the logical database and the physical database in difference view windows. There are ten difference view windows in the traditional flow.

- Instance Difference View window
- Instance Part Difference View window
- Instance Property Difference View window
- Net Difference View window
- Net Property Difference View window
- Pin Property Difference View window
- Pin-Swapping Difference View window
- Pin-Connection Difference View window
- Section-Swapping Difference View window
- RefDes-Swapping Difference View window

The following generic features apply to all of the above-mentioned difference view windows:

- The titlebar of every difference view window displays the name of the difference view, the design name corresponding to the logical Concept HDL schematic, and the layout name of the layout database to which it is being compared.

- Design Differences displays a difference view window only if differences exist between the schematic and the layout. If the logical design in the Concept HDL schematic and the physical design in the Allegro or SPECCTRAQuest layout do not have any differences, Design Differences displays this in a message box.
Each column in a difference view window identifies the information related to the differences between the logical and physical views while each row displays the differences.

Sometimes, a column in a window might display a partial value. If this happens, place the pointer on the column-header title and drag the column header outline to the right to display the full value.

Each difference view window lets you arrange all differences in an alphabetical order. For this, you need to click the column header corresponding to the column on which you want to sort properties.

You can highlight or dehighlight any instance, component, net, or pin in a Concept HDL schematic or an Allegro or SPECCTRAQuest layout.

**Differences View Windows: Constraint Manager Enabled Flow**

In the Constraint Manager enabled flow, besides the above difference view windows, two more difference view windows exist. These are Constraints Differences - Physical Difference View window and Constraints Differences - Logical Difference View window.

Constraints differences are displayed in the following format:

```
Net: <net_name>
```
Object differences are displayed in the following format:

- **<object> association**  (<new association>)  (<old association>) (*<original association>*)

- "Clearing" an object implies that all electrical constraints captured on the object have been deleted.

The **Summary** section displays the summary of constraint and object differences between the schematic and the board.

**Note:** For more information about Constraints Differences windows, see *Concept HDL User Guide* in CDSDoc.

### Physical Design View Window

The Physical Design View window displays the objects in the physical view of the design as hierarchical trees. To display the Physical Design View window, choose **Explore - Physical Design**.

There are three hierarchical trees, one each for components, nets and parts. By default, a hierarchical tree is not expanded. The root node of a component, net, or part hierarchical tree displays a number signifying their total number in the design. For example, **components=29** in the root node of the component tree signifies that there are 29 components in the design.

**Figure 5-7  Physical Design View Window: Unexpanded**

![Physical Design View Window](image)

### Logical Design View Window

The Logical Design View window displays the objects in the logical view of the design as hierarchical trees.
There are three hierarchical trees, one each for components, nets, and parts. By default, none of these trees are expanded. The root node of the component, net, or part hierarchical tree displays a number signifying their total number in the design. For example, nets=108 signifies that there are 108 nets in the design.

**Figure 5-8 Logical Design View Window: Unexpanded**

![Logical Design View Window: Unexpanded](image)

**Rearranging Windows**

If there are multiple open windows in Design Differences, you might like to rearrange them for better viewing. You can rearrange a window in any of the following ways:

1. Choose *Window - Cascade*. This command arranges all the active windows as a cascade. The active window appears at the top of the cascade and the titlebars of the other windows are visible beneath it like a cascade.

2. Choose *Window - Vertical Tile*. This command arranges all the active windows vertically (that is each window appears as a column in a single row table).

3. Choose *Window - Horizontal Tile*. This command arranges all the active windows horizontally (that is, each window appears as a row in a single column table).

4. Choose *Window - Arrange Icons*. This command arranges all the icons relating to active windows.

5. Choose *Window - Close All*. This command simultaneously closes all open windows.

**Using Design Differences**

**Viewing Any Files**

Multiple files are generated when you package a design. You can view any packaging file or any other file in the design from Design Differences. To view any file,
1. To display any file, choose *File - View File*. This displays the Select File dialog box.

2. Use the *Browse* button to navigate to the design directory containing the files you want to see.

3. Choose the required view from the list box containing the cell views of the design.

4. Choose the required file format (*.dat, *.log, *.txt, *.dif, or *.mkr) from the *Files of type* list box.

5. Click *Open* to display all the files corresponding to the file format you selected.

   The list of files under the selected view directory appears. For example, if you selected the *.mkr file format, the dessync.mkr and pxl.mkr files now appear in the list box.

6. Choose any file from the list box by highlighting the file.

   The name of the file you selected appears in the *File Name* box.

7. Click *Open* to view the file.

   or

   Click *Cancel* if you want to close the Select File dialog box without displaying the file.

**Viewing Errors**

You can view errors by either using the Message Log window or by viewing the dessync.log or pxl.log files. To view any file, refer to *Viewing Any Files*.

**Viewing the Logical Design**

You can display the objects in the logical view of the design as hierarchical trees.

➤ To view the logical design, choose *Explore - Logical Design*.

The Logical Design View window displays with the title `<design_name>(<view_name>)`. *Logical Design View Window: Unexpanded* represents a logical design window. You can expand the hierarchical list to view the details about components, nets, or parts.

A hierarchical tree can run into multiple levels. For example, the components tree in the logical design window is organized into six levels. To expand any level, you can do one of the following two steps:

- Click the + button to the left of the base node of the non-expanded level.
- Double-click the base node of the non-expanded level.
The Logical Design View Window: Expanded Component Tree figure on page 119 displays the expanded components tree. The numbers 1 to 6 represent the actions that you need to complete.

Figure 5-9 Logical Design View Window: Expanded Component Tree

1. Click the component tree node to list the reference designator identifying each component and the name of each part together with the PACK_TYPE property attached to it.
2. Click a component tree node to list the number of instances.
3. Click the number of instances node to display the information about the path and section number.
4. Click the tree node corresponding to the path and the section number to display the number of pins and properties attached to the component.
5. Click the tree node corresponding to the total pin number to display the pin name, pin number, and the net name.
6. Click the tree node corresponding to the total properties number to display the instance properties.
See Viewing the Hierarchical List of Components on page 122 for a detailed procedure of expanding components in a hierarchical tree.

Viewing the Physical Design

You can display the objects in the physical view of the design as hierarchical trees.

➤ To view the physical design, choose Explore - Physical Design.

Physical Design View Window: Unexpanded represents a logical design window displayed by running the above command. The Physical Design View window is displayed in the title <design_name>(<board_name>). You can expand the hierarchical list to view the details about components, nets, or parts.

An example of how the hierarchical net tree is expanded in the physical design window appears in Physical Design View Window: Expanded Net Tree on page 121. The numbers 1 to 5 represent the actions that you need to complete.
Figure 5-10  Physical Design View Window: Expanded Net Tree

1. Click the net tree base node to display the list of all nets.
2. Click the tree node corresponding to a particular net to display the number of net connections and properties and the logical net name.
3. Click the node displaying the number of connections to display the pin name, pin number, reference designator, and the part to which the net is attached.
4. Click the tree node corresponding to a connection to display the hierarchical logical net name.
5. Click the node displaying the number of connections to display the net properties.

See Viewing the Hierarchical List of Nets on page 122 for the detailed procedure of expanding components in a hierarchical tree.

Viewing the Differences in a Text Editor

You can view the differences in a text editor by sending the differences generated in VDD to a text file.
To view the differences in a text editor, choose File - Output Differences.

The differences corresponding to the difference view window that is currently active are displayed in the default text editor. You can either edit or print these differences.

Viewing Hierarchical Trees

You can view any hierarchical tree by expanding its individual levels.

Viewing the Hierarchical List of Components

1. Click the components tree node to display the list of reference designators identifying each component and the name of each part together with the PACK_TYPE property attached to it.

2. Click the tree node corresponding to a specific component to display the total number of instances related to the component.

3. Click the <total number of instances> tree node to display the path and section number related to all instances of the component.

4. Click the tree node corresponding to the path and section number (displayed in the last step) to display the number of pins and properties attached to the component. The hierarchical logical path of the component is also displayed.

5. Click the tree node corresponding to the [pins = <total number of pins>] tree node to display the pin name, pin number, and net name.

6. Click the [properties = <total number of properties>] tree node attached to the component to display a list of all instance properties attached to the component.

See Logical Design View Window: Expanded Component Tree on page 119 for a detailed diagram that implements the above-mentioned steps.

Viewing the Hierarchical List of Nets

1. Click the tree node corresponding to [nets = <total number of nets>] to display the list of all nets in the alphabetical order.

2. Click the tree node corresponding to a specific net to display the number of net connections, the number of properties, and the hierarchical, logical net name.
3. Click the tree node corresponding to \([connections = \text{<total number of connections>}]\) to display the pin name, the pin number, the reference designator, and the part to which the net is attached.

4. Click the tree node corresponding to each individual connection in the tree to display the hierarchical logical pin name.

5. Click the tree node corresponding to \([properties = \text{<total number of properties>}]\) for this net to display the net properties.

See Physical Design View Window: Expanded Net Tree on page 121 for a detailed diagram that depicts the above-mentioned steps.

**Viewing the Hierarchical Listing of Parts**

1. Click the tree node corresponding to \([parts = \text{<total number of parts>}]\) to display the list of all the parts in the design.

2. Click the tree node corresponding to one specific part to display the total number of components of the part, the total number of pins in the part, and the total number of properties attached to the part.

3. Click the tree node corresponding to \([components = \text{<total number of components>}]\) to display the reference designators identifying the components.

4. Click the tree node corresponding to any reference designator to display the total number of instances and the total number of properties attached to the reference designator.

5. Click the tree node corresponding to \([instances = \text{<total number of instances>}]\) to display the part, the section number, and the part name for each of the instances of the part.

6. Click the tree node corresponding to any instance to display the total number of pins, the total number of properties, and the canonical path name of the instance.

7. Click the tree node corresponding to any pin attached to the selected instance to display the pin name, the pin number, and the net name corresponding to the instance.

8. Click the tree node corresponding to the properties of the instance to display the instance properties.

9. Expand the tree node at the \([pins = \text{<total number of pins>}]\) level to display the pin names of the part.
Loading the Design Views

Loading the Concept HDL Schematic

1. To load the Concept HDL schematic, choose *File - Load Concept Schematic*.

   The Select Packaged View To Compare dialog box appears listing the packaged views that you can choose.

   ![Select Packaged View To Compare Dialog Box](image)

2. If you click *OK* without highlighting the packaged view that you want to compare, a Design Differences window appears with the Caution symbol. This window displays the warning that you have not selected any packaged view.

   Design Differences repackages the updated schematic design, reloads the logical view from the updated schematic, and displays a window with the message “Reload schematic has successfully completed.”

3. Click *OK*.

   The difference view windows are displayed. These windows list any differences that were found between the regenerated packaged view of the Concept HDL schematic and the Allegro or SPECCTRAQuest layout view.

Loading the Allegro Layout

1. To load the Allegro layout, choose *File - Load Allegro Board.*
The Select Board File To Compare dialog box appears listing the board files that you can choose.

**Figure 5-12  Select Board File To Compare Dialog Box.**

![Select Board File To Compare](image)

2. In the *layout* view, select the board file that you want to compare with the packaged view in the schematic and click OK.

   **Note:** You may click Cancel if you do not want to compare any board file in the layout view with the packaged view in the schematic.

Design Differences re-extracts the physical layout design, reloads the *physical* view from the layout, and displays a window with the message “Reload Allegro Board has successfully completed.” Clicking OK on this window displays the difference view windows. These windows list any differences found between the regenerated Allegro layout physical view and the packaged logical view of the Concept HDL schematic.

**Querying a Design**

**Querying for a new instance, component, net, pin, or property**

1. To display the Query Design dialog box, choose *Explore - Query Design*.

   The *Query Design Dialog Box* figure on page 126 appears.
2. Click **New**.

   The Add Query dialog box appears. You can use this dialog box to search for any instance, component, net, or pin in the schematic or the board.
3. Enter the name of the instance, component, net, pin, or property that you want to search for in the *Query Name* field.

4. Depending on whether you want to select the object in the logical design or in the physical design, click the *Schematic* or *Board* radio button.

5. In the *Find What* group box, specify whether you are searching for instance, component, net, or pin by clicking the respective radio button.
6. In the *Search Type* group box, select either the *Match Case* radio button or the *Match the whole word only* radio button. If the instance name, component name, net name, pin name, or property name you are searching for is case-sensitive, select the *Match Case* radio button. If you want a whole-word search, select the *Match the whole word only* radio button.

7. In the *Search Qualifier* group box, select an option (By Part Name, By Ref Des, By Net Name, by Property Name, or by Cname) and type in the specific part, reference designator, net name, property name and value, or the canonical path you are searching for.

8. Click *OK*.

   The Query Design dialog box reappears with the *Query Name* field showing the name of the instance, component, net, pin, or property you are querying.

9. Click *Find*.

   The *Query Board* - *<query name>* or *Query Schematic* - *<query name>* window appears with a list of all the instances, components, nets, or pins in the logical or physical design that matches the query.

10. To further expand the tree and display the specific location and properties attached to the object, click the tree node corresponding to an object in this list.

**Example**

For example, to search for all the parts in the schematic with the DES property value of **F6**, display the Add Query dialog box and follow the steps below:

1. Type these selections:
   
   | **Query Name** | DES |
   | **In Design**  | Schematic |
   | **Find What**  | Instance |
   | **Search Type** | Match the case |
   | **Search Qualifier** | By Part Name |
   | **By Property: DES Value: F6** |

2. Click *OK* in the Add Query dialog box. The Query Design dialog box appears with DES in the *Query Name* field.

3. Click *Find*. 
The *Query Logical Design - DES* window appears listing all the parts in the schematic that have the DES property value of F6.

**Querying for another instance, component, net, pin, or property**

1. To display the Edit Query dialog box in which you can edit an existing query, click *Edit* in the Query Design dialog box. The Edit Query dialog box appears.
Figure 5-15 Edit Query Dialog Box

![Edit Query Dialog Box](image)

The Edit Query dialog box has the same selection options and check boxes as the Add Query dialog box.

2. You can now make any changes in the query. (Steps similar to the steps 3-8 for Querying for a new instance, component, net, pin, or property on page 125).
Highlighting and Dehighlighting Objects

Steps to follow before highlighting or dehighlighting objects

Before highlighting an object in a Concept HDL schematic and its corresponding graphical element in the Allegro or SPECCTRAQuest layout, you need to select a difference displayed in any of the following windows or dialog boxes:

- Difference view window
- Query Schematic and Query Board windows
- Preview ECO on Allegro Board or Preview ECO on Schematic dialog box

**Note:** Neither the menu command nor the alternative steps given below will work unless you have selected a difference in any of the above-mentioned windows.

Highlighting Objects

To highlight the object source corresponding to the selected difference:

- Choose *Display - Highlight Source* from the Design Differences menu bar.

The Design Differences tool automatically opens up the corresponding page in the Concept HDL schematic design and highlights its source. If a match for the graphical element corresponding to the object being highlighted exists in the Allegro or SPECCTRAQuest layout, the object is also highlighted.

You can use the following alternative steps to highlight an object.

1. Position the pointer in any of the following windows or dialog boxes:

- Difference view window
- Query Schematic and Query Board windows
- Preview ECO on Allegro Board or Preview ECO on Schematic dialog box

2. Choose the instance, component, net, or pin difference whose source you need to highlight.

3. Click the right mouse button on the selected object.

   or

   Double-click the selected object.
A pop-up menu with two commands, *Highlight Source* and *Dehighlight Source*, appears.

4. Choose *Highlight Source*.

The selected object is highlighted in the logical view. Its corresponding graphical element in the physical view is also highlighted if a corresponding match exists.

**Dehighlighting Objects**

**To dehighlight using the menu command**

To dehighlight the object source corresponding to the difference you selected:

➤ Choose *Display - Dehighlight Source* from the Design Differences menu bar.

Design Differences automatically opens up the corresponding page in the Concept HDL schematic design and dehighlights its source. Its corresponding graphical element in the Allegro or SPECCTRAQuest layout also gets dehighlighted if a corresponding match exists.

**Alternative steps to dehighlight (without using the menu command)**

1. Position the pointer in any of the three windows listed below:
   - Difference view window
   - Query Logical Design or Query Physical Design window
   - Preview ECO on Allegro Board or Preview ECO on Schematic dialog box

2. Choose the instance, component, net, or pin difference whose source you need to highlight.

3. Click the right mouse button on the selected object.

   or

   Double-click the selected object.

   A pop-up menu with the *Highlight Source* and *Dehighlight Source* options appears.

4. Choose *Dehighlight Source*.

The selected object is dehighlighted in the logical view. Its corresponding graphical element in the physical view is also dehighlighted if a corresponding match exists.
Regenerating Difference Views

➤ To repackage the schematic, update the schematic view (logical view), and regenerate the differences, and choose File - Load Concept Schematic.

-or-

➤ To re-extract differences from the Allegro or SPECCTRAQuest layout, update the layout view (physical view), regenerate the differences, and choose File - Load Allegro Board.

Note: In case you change the schematic or board while in VDD, you can view the effect by reloading the schematic or board.

Previewing ECO on Allegro Board

The Preview ECO on Allegro Board dialog box displays the list of the connectivity changes and property changes that need to be made on the physical view to update the layout and synchronize the layout database with the Concept HDL schematic design.

➤ To display the Preview ECO on Allegro Board dialog box, choose the Sync - Update Allegro Board command from the Design Differences menu bar.

Previewing ECO on Schematic

You can use the Preview ECO on Schematic dialog box to list the properties, instances, or nets that need to be modified in the logical view to update the schematic and to synchronize the Concept HDL schematic design with the layout database.

➤ To display the Preview ECO on Schematic dialog box, choose the Sync - Update Schematic command from the Design Differences menu bar.

Synchronizing Difference Views

You synchronize the difference views by accepting or rejecting ECO changes in the schematic and the layout. ECO changes are often made in the schematic or the layout after the initial transfer of packaging information from the schematic to the layout. You can preview ECOs and use the information contained in them to bring the schematic and the layout in sync.

Synchronizing the Board Layout

1. Choose Sync - Update Allegro Board from the Design Differences menu bar.
The Preview ECO on Allegro Board dialog box appears with the list of property and connectivity changes to be made to the layout.

**Figure 5-16 Preview ECO on Allegro Board Dialog Box**

2. By default, the connectivity or the property changes, if any, are forwarded to the Allegro board layout. If you do not want to forward either the connectivity changes or the property changes to the Allegro board layout, clear the **OK** check box under the relevant list.

   **Note:** If connectivity changes or property changes do not exist, the check box corresponding to them is grayed out.

3. Click the **OK** button to update the layout with the listed connectivity and property changes.
The Message log in the Design Differences window is updated. A message box appears asking if you want to update difference views.

4. Click Yes.
   A message box appears stating that the Allegro board has been successfully reloaded.

5. Click OK.
   A message box appears stating that no differences exists between the board and the schematic.

6. Click OK to close the message box.

**Synchronizing the Concept HDL Schematic**

1. Choose *Sync - Update Concept Schematic* from the Design Differences menu bar.
   The *Preview ECO on Schematic Dialog Box* on page 136 appears with two list boxes containing the lists of property and connectivity changes to be made to the Concept HDL schematic.
2. By default, the property and connectivity changes, if any, are fed back to the schematic. If you do not want to backannotate the connectivity changes to the Concept HDL schematic, clear the OK check box under the Connectivity Changes list box. This will not launch Design Association to feed back the property changes to the schematic.

-or-

If you do not want to launch Packager-XL to backannotate the property changes to the Concept HDL schematic, clear the OK check box under the Property Changes list box.

**Note:** By default, the check boxes for property changes and connectivity changes are selected. If there are no connectivity changes or property changes, then the check box corresponding to them are grayed out.
The Message log in the Design Differences window is updated and the Import Physical dialog box is displayed.

3. Click OK.

A Progress Window appears mentioning that design is netlisted and being fed back. Finally a message box appears asking whether you want to see Packager results.

4. Click No.

The Control is passed back to Design Differences, which displays a message that schematic has successfully loaded.

5. Click OK.

Packager-XL runs in the feedback mode and updates the packager files. Changes are also made to the Concept HDL schematic. A message box appears displaying the message that the schematic and the section_swapped2.brd board file are in sync.

6. Click OK to close the message box.

Comparing Differences between Schematics and Boards

For a given object, such as net, instance, or part, you can compare the differences between the logical view and the physical view. These differences are returned in a difference view window. For example, net differences are returned in the Net Difference window.

Comparing Net Differences

You can compare net objects to verify if they exist in the logical and physical views. To compare net objects:

➤ Choose Difference - Net from the Design Differences menu bar.

The Net Difference window displays the differences between the nets in the logical and physical views. These differences are displayed in a tabular format. A difference in net occurs when you have added or deleted a net from the schematic or the layout.

Note: If the logical and physical views do not have any differences, a message box appears stating that differences do not exist.

Comparing Instance Differences

You can compare instances to verify if differences exist in the logical and physical views. To compare instances:
Choose *Difference - Instance* from the Design Differences menu bar.

The Instance Difference window displays the differences between the instances in the logical and physical views. These differences are displayed in a tabular format. A difference in instance occurs when you have added or deleted an instance from the schematic or the layout.

**Comparing Instance Part Differences**

You can compare instance parts to verify if differences exist in the logical and physical views. A difference in an instance part occurs when there is:

- A **PACK_TYPE** property change
- A ptf file mapping change

To display the instance part differences,

➤ Choose *Difference - Instance Part* from the Design Differences menu bar.

The Instance Part Difference window appears. This window displays the differences between the instance parts in the logical and physical views. These differences are displayed in a tabular format.

**Comparing Pin-Net Connection Differences**

Pin-net differences occur when you rewire nets, add instances or nets, or delete instances or nets in either the schematic or the layout. To view the connectivity differences between the logical and physical views in a tabular format, display the pin-net connection differences in the Pin-Net Connection Difference window.

To display the pin-net connection difference,

➤ Choose *Difference - Pin Connection* from the Design Differences menu bar.

The Pin-Net Connection Difference window appears. The differences between pins and nets are displayed in a tabular format.

**Comparing Instance Property Differences**

To display the instance property differences between the logical and physical views:

➤ Choose *Difference - Inst Property* from the Design Differences menu bar.
The Instance Property Difference window displays the instance property differences between the logical and the physical views in a tabular format.

**Comparing Pin Property Differences**

You can have pin property differences between the logical and physical views because of the following two reasons,

1. You have added, modified, or deleted a property that is attached to a pin in the schematic or layout.

2. You might not have specified the pin properties that need to be fed back to the \texttt{pxlba.txt} file. A missing pin property in the \texttt{pxlba.txt} file would give a false impression that the pin property is missing on the schematic.

To display the pin property differences between the logical and physical views,

➤ Choose **Difference - Pin Property** from the Design Differences menu bar.

The Pin Property Difference View window appears. This window lists the pin property differences between the logical and physical views.

**Note:** To control the pin properties that are transferred from the schematic to the layout and back from the layout to the schematic, use the Property Flow Setup dialog box.

**Comparing Net Property Differences**

You can have net property differences between the logical and physical views because of the following two reasons:

1. You have added, modified, or deleted a property that is attached to a net in the schematic or layout.

2. You might not have specified the net properties that need to be fed back within the \texttt{pxlba.txt} file. A missing net property in the \texttt{pxlba.txt} file incorrectly suggests that the net property might be missing on the schematic.

You can display the net property differences in the Net Property Difference window. To display the net property differences,

➤ Choose **Difference - Net Property** from the Design Differences menu bar.

The Net Property Difference window appears. This window displays the differences in net properties between the logical and physical views in a tabular format.
Note: To control the pin properties that are transferred from the schematic to the layout and back from the layout to the schematic, use the Property Flow Setup dialog box.

Comparing Pin-Swapping Differences

To view the pin-swapping differences between the logical and physical views,
➤ Choose Difference - Pin Swapping from the Design Differences menu bar.

The Pin-Swapping Difference window displays the pin-swapping differences between the logical and physical views in a tabular format.

Comparing Section-Swapping Differences

You might have different sections in the schematic and the board. These sections might have been swapped (that is, interchanged with each other). For example, a section with the schematic value 6 might be assigned the value 4 on the board. You can display the section-swapping differences in the Section-Swapping Differences window.

To display the section-swapping differences between the logical and physical views,
➤ Choose Difference - Section Swapping from the Design Differences menu bar.

The Section-Swapping Difference window displays the section-swapping differences between the logical and physical views in a tabular format.

Note: Design Differences uses the physical section transformations file, pstsecx.dat, to reassign a logical part from an old physical section to a new physical section. This file contains the list of section numbers that have been changed. The file lists the old and new values of the changed section numbers.

Comparing Refdes Differences

If you have changed the LOCATION or the CDS_LOCATION property in the schematic or have renamed a reference designator in the layout, refdes swapping differences will exist between the schematic and the layout.

To display the differences in the reference designators between the logical and the physical views,
➤ Choose Difference - RefDes Swapping from the Design Differences menu bar.

The Refdes Difference window displays the section-swapping differences between the logical and physical views in a tabular format.
Filtering Differences Between Schematics and Boards

You can filter the nets, instances, or properties that you do not need or do not want to synchronize.

To filter the differences,

➤ Choose Difference - Filter Options from the Design Differences menu bar.

The Filter Options for Difference dialog box appears. It has five tabs: Instance Property, Net Property, Pin Property, Instance, and Net. To filter any differences, select the respective tab.

Figure 5-18 Filter Options for Differences Dialog Box

Note: Filter options let you control the display of differences. You cannot control the backannotation of data using the Filter Options for Difference dialog box.
Filtering Instance Properties

You can filter instance properties using the following steps:

1. Choose *Difference - Filter Options* from the Design Differences menu bar.
   The Filter Options for Difference dialog box appears. The Instance Property tab is selected by default.

2. Choose the net properties you need to filter and move them from the *Available Net Properties* list box to the *Ignored Net Properties* list box or vice versa.

3. Click *OK*.

The instance properties selected in the *Ignored Instance Properties* list box are ignored.

Filtering Net Properties

You can filter net properties using the following steps:

1. Choose *Difference - Filter Options* from the Design Differences menu bar.
   The Filter Options for Difference dialog box appears.

2. Select the *Net Property* tab.

3. Select the net properties you need to filter and move them from the *Available Net Properties* list box to the *Ignored Net Properties* list box or vice versa.

4. Click *OK*.

The net properties selected in the *Ignored Net Properties* list box are ignored.

Filtering Pin Properties

You can filter pin properties using the following steps:

1. Choose *Difference - Filter Options* from the Design Differences menu bar.
   The Filter Options for Difference dialog box appears.

2. Select the *Pin Property* tab.

3. Select the pin properties you need to filter and move them from the *Available Pin Properties* list box to the *Ignored Pin Properties* list box or vice versa.

4. Click *OK*.
The pin properties selected in the *Ignored Pin Properties* list box are ignored.

**Filtering Instances**

You can filter instances using the following steps:

1. Choose *Difference - Filter Options* from the Design Differences menu bar.
   
   The Filter Options for Difference dialog box appears.

2. Select the *Instance* tab from this dialog box.

3. Select the instances you need to filter and move them from the *Available Instances* list box to the *Ignored Instances* list box or vice versa.

4. Click *OK*.

The instances selected in the *Ignored Instances* list box are ignored.

**Filtering Nets**

You can filter nets using the following steps:

1. Choose *Difference - Filter Options* from the Design Differences menu bar.
   
   The Filter Options for Difference dialog box appears.

2. Select the *Net* tab in this dialog box.

3. Select the nets you need to filter and move them from the *Available Nets* list box to the *Ignored Nets* list box or vice versa.

4. Click *OK*.

The instances selected in the *Ignored Nets* list box are ignored.
Using Design Association

Overview

The Design Association tool is an important component of the Design Synchronization toolset. It allows you to update the connectivity changes made in the layout to the schematic. Design Association provides an intuitive user interface, which displays markers to all connectivity changes. You can select any marker and use it to update the Concept HDL schematic.

The Design Association tool performs the following three tasks:

1. Communicates with the Concept HDL schematic through Concept HDL SKILL
2. Executes the functions related to the Actions generated for connectivity markers
3. Updates the Concept HDL schematic design

How Design Association Fits in the Front-to-back Flow

When creating concurrent designs, you can transfer the packaging information from the schematic to the layout and continue to make changes both to the schematic and the layout. You can synchronize these changes using Design Synchronization tools. For details about how Design Association fits in the front-to-back flow, see Design Association Tool in the Front-to-Back Flow on page 145.

Design Association uses a file generated by VDD, dessync.mkr, which captures the connectivity change information and guides you in updating the schematic.

The property changes are made to the schematic using the Design Differences tool.
Figure 6-1  Design Association Tool in the Front-to-Back Flow

- **Concept HDL**
  - Schematic
  - Property changes / backannotation

- **Packager-XL (Export Physical)**
  - PXL files (3 pst*.dat files)

- **Netrev**

- **Design Association**
  - Dessync.mkr
  - PXL files (*view.dat)

- **Packager-XL (Import Physical)**
  - Feedback files (4 *view.dat files)

- **Genfeedformat**

- **Allegro or SPECCTRAQuest**
  - Board files
  - Backward flow
  - Front End
  - Front-to-Back
  - Back End

- **Forward Flow**
  - Inputs for Design Differences

- **Backward flow**
Design Association Functions

The Design Association tool:

- Helps you to navigate through a Concept HDL schematic and run a design editing session where you can update and synchronize the logical Concept HDL schematic design with the corresponding physical layout drawing.

- Guides you to the individual pages of the schematic and prompts you with the connectivity changes and design changes that need to be fed back based on the changes in the layout.

Understanding Markers and Actions

Markers

Markers record the information about the connectivity changes in the layout. This information is used by Design Association to do an update action on the Concept HDL schematic design.

Dessync Marker File

The Design Differences tool creates the dessync marker file. This file contains the list of connectivity changes that you need to make in the Concept HDL schematic to synchronize it with the physical layout view. This file resides in the packaged view of the design that you have loaded in your Concept HDL schematic.

Actions

To synchronize the Concept HDL schematic design with the Allegro or SPECCTRAQuest layout changes, you need to run actions corresponding to the markers in the Markers list box. You can use the Design Association tool to start an action.

When you start an action, the Design Association tool:

- Transfers the property information (object properties, net names, and so on) stored in the dessync.mkr input file to the Concept HDL schematic and updates the schematic design.

- Reflects the execution status of the action in the check box corresponding to the marker.
Launching and Exiting Design Association

Overview

You launch Design Association from the Concept HDL schematic editor or from Design Differences. Before you start the schematic design, expand Concept HDL.

Note: If you open Design Association without expanding the design, Concept HDL displays a warning message. You are also allowed to expand the design.

Launching from the Concept HDL Schematic

1. Open the Concept HDL schematic design.
2. To expand the design, choose Tools - Expand Design from the Concept HDL menu bar.
   The Design Association Window figure on page 150 appears.

Launching from the Design Differences Tool

1. Launch the Design Differences tool.
2. Choose Sync - Update Concept Schematic from the Design Differences menu bar.
   The Preview ECO on Schematic Dialog Box figure on page 148 appears.
3. Select the **Click OK button to launch Design Association to feedback connectivity changes to schematic** check box.

4. Click **OK** on the Preview ECO on Schematic dialog box.

   The **Design Association Window** figure on page 150 appears.

**Exiting Design Association**

➢ To exit from Design Association, choose **File - Exit** from the menu bar.

If the marker file has changed, Design Association displays a window that helps you save the Concept HDL schematic. If you click **OK**, all the modified pages of the Concept HDL...
schematic are saved. You can also save the marker file by using Design Association and use the file to update the changes to the schematic.

**Design Association User Interface**

When you launch Design Association, it displays a window containing the list of markers. By default, the Design Association window does not display details about markers.
Main Window

Figure 6-3  Design Association Window

The Design Association window has a titlebar that displays the name of the project file that you loaded in Concept HDL. For example, in the Design Association Window figure on page 150, the titlebar displays the name of the project file as atm. The window also has a menu bar, a Markers list box, a status bar, and the following three buttons: Execute, Detail, and Help.

You can use the Execute button to run the action associated with the marker. You can expand the Design Association window to display the Detail section by clicking the Detail button. The
*Detail* button acts as a toggle button. If you have expanded the window, you can click the *Detail* button to display the default main window.

The Design Association window helps you:

- Execute any of the Design Association menu commands
- Select any of the actions listed in the *Markers* list box and start the function associated with the action
- Filter the actions through the Filter/Select dialog box
- View the detailed information associated with each marker
- Update the information corresponding to the synonyms of the net for a selected marker, location, or the nets in the *Markers* list box

**Detail Window**

You can expand the Design Association window to display the *Detail* section. To expand the Design Association window,

➤ Click the *Detail* button.

The Design Association window expands as displayed in the Design Association Window: Expanded figure on page 152.
The Detail window displays detailed information about the markers listed in the Markers list box. You can select any marker from the Markers list box. When a marker is selected, the check box associated with the marker is highlighted. The detailed information corresponding to the selected marker appears in the Detail window. The Detail window also displays the execution status of actions. When an action is executed, the status is updated accordingly. If the action fails, it displays the reason for the failure of the action.
Markers List Box

The *Markers* list box provides the following:

- A static field to show `<Marker number><(Total number of markers)>`. For example, [Design Association Window on page 150](#) displays the following value: *Markers: 1(3)*. This signifies that the selected marker is the first marker in a list of three markers.

- A list of markers that you can expand as hierarchical trees. Each marker corresponds to an action required for updating the Concept HDL schematic. For more information about how to expand a hierarchical tree, see [Displaying a Hierarchical Tree on page 158](#).

How Markers are Displayed

Markers are displayed in the following order:

- All markers are sorted by nine different *Action Types*.
  - **Note**: Each marker corresponds to an action used by Design Association to update the Concept HDL schematic design.

- When a marker is unexpanded, it shows the execution status of the action and the action type to be executed. A check box to the left of each marker displays the execution status of the action.

- When an action associated with a marker has not been executed and you select a marker, Design Association automatically navigates to the corresponding location in the Concept HDL schematic. In addition for [Add Net To Pin, Delete Net From Pin, or Replace Net on Pin](#) action types, it highlights the pin-net connection and for the [Add Instance or Delete Instance](#) action types, it highlights the instance.

- By default, the marker list is unexpanded. You can choose the *View - Expand Markers* command from the Design Association menu bar to see a hierarchical tree view of markers. If you again choose the *View - Expand Markers* command, the marker list appears collapsed.

- When you expand any marker, Design Association displays detailed information about the objects in the Concept HDL schematic on which it will operate for the selected marker. You can select any tree node in the marker list and update the schematic with the action specified by the marker.

- Navigating to an object results in changing its parent location node in the tree to the checked state. You can expand each marker by clicking its tree node. Each marker, when fully expanded, displays the action type, the full drawing path of the location, the instance port, the net name, and synonyms.
**Note:** You can control the display of markers in the tree control based on the action type, execution status, and the short message string.

**Execution Status of an Action**

The check box next to each tree node corresponding to an action changes color based on the execution status of the action. The following figure describes the meaning of each colored check box in Design Association:

**Table 6-1 Execution Status of an Action**

<table>
<thead>
<tr>
<th>Color</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Black</td>
<td>The action was not executed.</td>
</tr>
<tr>
<td>Gray</td>
<td>The action cannot be executed. This is valid only for the Add Instance action type.</td>
</tr>
<tr>
<td>Red</td>
<td>The action was unsuccessfully executed.</td>
</tr>
<tr>
<td>Blue</td>
<td>The action was successfully executed.</td>
</tr>
<tr>
<td>Magenta</td>
<td>Locations added with the Action - Add Location command are preceded by magenta check boxes.</td>
</tr>
</tbody>
</table>

**Action Types**

The Design Association tool lists nine action types. Each action types does an action on a particular marker type. For example, the Action Type - Delete an Instance deletes an instance from the Concept HDL design.

The following section describes the function of each action type.

**Delete Instance Action Type**

The Delete Instance action type deletes an instance from the Concept HDL design.

The Delete Instance marker in the Markers list box indicates the drawing in your Concept HDL design, where the instance to be deleted is located. You need to delete this instance for synchronizing the Concept HDL schematic and the Allegro or SPECCTRAQuest layout.
Add Instance Action Type

The Add Instance action type adds an instance that is present in Allegro or SPECCTRAQuest to your Concept HDL design. The Add Instance action type adds the instance and also does the following tasks:

- Attaches properties to the instance
- Makes net-stub connections
- Attaches pin properties
- Attaches net properties

Note: An Add Instance marker can have multiple locations. Therefore before you add an instance, you need to select the location where you want the instance to be placed in the Concept HDL schematic. If you do not select any location, Design Association will select the first location. You can later recompute the locations or select a page in the Concept HDL schematic and define it as the location for adding instances.

Delete Pin Net Action Type

The Delete Pin Net action type deletes a specified net from a pin within your Concept HDL design. You need to delete the specified pin-net connection for synchronizing the Concept HDL schematic and Allegro or SPECCTRAQuest layout.

Add Pin Net Action Type

The Add Pin Net action type adds a pin-net connection to an instance in your Concept HDL design. You need to add this pin-net connection for synchronizing the Concept HDL schematic design with the Allegro or SPECCTRAQuest layout design.

Replace Pin Net Action Type

The Replace Pin Net action type replaces a pin-net connection in your Concept HDL design.

You use this action type to replace a pin-net connection for synchronizing the Concept HDL schematic with the Allegro or SPECCTRAQuest layout design.
Add Series Terminator Action Type

The Add Series Terminator action type, also known as Add Series Term, adds a series terminator to the net on the given pin.

Besides adding the series terminator, the Add Series Terminator action type does the following tasks:
- Attaches properties to the instance
- Makes net-stub connections
- Attaches pin properties
- Attaches net properties

Add Shunt Terminator Action Type

The Add Shunt Terminator action type, also known as Add Shunt Term, adds a shunt terminator to the net on the given pin.

**Note:** You can apply the Add Shunt Term action type on Pull Down, Shunt RC, Power Diode, Ground Diode, Dual Diode, and Thevnin shunt terminators. You can add multiple instances of the shunt terminator using the Add Shunt Term action type.

In addition to adding the shunt terminator, the Add Shunt Terminator action type does the following tasks:
- Attaches properties to the instance
- Makes net-stub connections
- Attaches pin properties
- Attaches net properties

Replace Instance Action Type

The Replace Instance action type replaces an existing instance on your Concept HDL design with a new instance.

You need to replace this instance for synchronizing the Concept HDL schematic and the Allegro or SPECCTRAQuest layout.

The Replace Instance action type does the following tasks:
Design Synchronization and Packaging User Guide

Using Design Association

- Deletes the existing component
- Adds the new instance
- Attaches properties to the instance
- Makes net-stub connections
- Attaches pin properties
- Attaches net properties

You can do the **Replace Instance** action in two modes, Automatic and Interactive. In the Automatic mode, Design Association checks if a new component can physically fit in the same space occupied by the existing instance and routes the pin-net connection. If the new component can fit in the same space as the existing component, Design Association replaces the instance. Otherwise, you are prompted to place the instance in another location and the connection is completed through the **Connect by Name** command.

In the Interactive mode, you can select the place in Design Association for adding instances. If you want to add the instance on a different page, you can select the location in the Concept HDL design where you want to add the instance. If you do not select any location, Design Association selects the first location by default.

**Change Part Action Type**

The **Change Part** action type changes the property on an existing instance on your Concept HDL design so that the physical part of the instance is synchronized with the Allegro or SPECCTRAQuest layout.

**Using Design Association**

You can use Design Association to do the following procedures described in this section:

- **Displaying a Hierarchical Tree** on page 158
- **Expanding a Marker** on page 158
- **Starting an Action** on page 159
- **Adding Locations, Nets, Instances, and Terminators** on page 163
- **Backannotating to Concept HDL** on page 166
- **Changing Parts** on page 167
Opening and Saving the Markers File on page 172

Displaying a Hierarchical Tree

When Design Association appears for the first time, the Markers list box shows the unexpanded markers, which display only the names of the corresponding action types. To display a hierarchical tree, you have to expand the marker.

1. To expand a marker, choose View - Expand Markers from the Design Association menu bar.

   The Design Association tool expands all the markers. A tree control appears with a tree node (+ sign) next to each marker.

2. Click the tree node next to any marker to expand the marker and display more details on the specific marker. For more details about expanding a marker, see Expanding a Marker on page 158.

Design Association automatically opens the drawing page corresponding to the marker in the Concept HDL design. It also highlights a section in which any instance needs to be added, or the section where a pin-net connection needs to be made or replaced, or a section from where an instance or the pin-net connection needs to be removed.

Expanding a Marker

1. Expand the tree node corresponding to an unexpanded marker.

   The full drawing path of the instance corresponding to the marker appears. You can add the instance in this expanded path.

   Note: The first tree node constitutes the best location. If Design Association is not able to find any such location, the bitmap associated with the action turns red to mark the action as unexecutable.

2. Expand the tree node corresponding to the drawing path at that location to see the instance ports. The Delete Instance and Add Instance action types can have multiple instance ports.

3. Expand the tree node corresponding to the instance ports to see the nets (signals) connected to the instance ports.

4. Click the net name.

   Design Association finds the synonyms of the net and updates the Design Association window with the synonyms of the net.
5. Select any of the synonyms or aliases.

Design Association opens the corresponding drawing in the Concept HDL schematic and highlights the corresponding location. See Design Association Window: Expanded on page 152 to understand how a marker expands. The following diagram shows a sample synonym GND\G highlighted in Concept HDL.

**Figure 6-5 Synonym Highlighted by DA in Concept HDL**

![Synonym Highlighted by DA in Concept HDL](image)

**Starting an Action**

To synchronize the Concept HDL schematic design with the Allegro or SPECCTRAQuest layout changes, you need to start actions corresponding to the markers in the Markers list box.

There are two modes in which you can start actions.

- Interactive mode
- Automatic mode

In the Interactive mode, Design Association lets you chose the location for the new instance in the Concept HDL design. In the Automatic mode, Design Association automatically starts all the actions corresponding to the markers in the Markers list box. To start a large number of actions, you can use the Automatic mode. You can select the mode in the Setup window (also called the Property Sheet).

To display the Setup window,

➢ Choose *Options - Set Up* from the Design Association menu bar.

The Property Sheet on page 160 appears.
Figure 6-6 Property Sheet

1. The default mode is Interactive. If you want to select the Automatic mode, click the Automatic radio button.

2. The default page border for adding new instances is a size page. To change the page border, type the required drawing page size in the Page Border field and click OK.

You have changed the mode setting. All marker changes will now be automatically executed. If the page corresponding to the location of a marker does not exist, the page will be created with the page border defined in the Page Border field.
Running an Action for a Selected Marker

1. Select the marker whose action you need to start from the Markers list box.

2. If you need to display more information about the marker, expand it.
   
   Design Association automatically opens the corresponding drawing page in the Concept HDL schematic design.

3. To start the action, choose Action - Execute from the Design Association menu bar.
   
   or
   
   Click the Execute button.  

Depending on the mode you select in the Property Sheet figure on page 160, the action corresponding to the marker is automatically executed or interactively executed. The check box next to the marker also changes to reflect the execution status of the action.

Note: It is possible to run multiple actions simultaneously. See Running Multiple Actions Simultaneously on page 161 for more information about executing multiple actions.

Running the Action Again

If you have done a Delete or Undo action in the Concept HDL schematic and need to run the action again, follow the following steps:

1. Select the marker associated with the action.

2. Clear the marker by choosing Action-Clear Status.

3. Once the marker is cleared, follow the steps 1-3 as mentioned in the procedure Running an Action for a Selected Marker on page 161 to run the action again.

Running Multiple Actions Simultaneously

You can start multiple actions simultaneously by using the Ctrl and Shift keys. Before you start any action that adds any instance, ensure that you have selected the page border in the Property Sheet on page 160.

1. Select all the markers in the Markers list box by using the Shift or Control key.

   Note: The Shift key is used to select markers in succession. For example if you select the third marker and keeping the Shift key pressed, select the 17th marker, all markers beginning from the third to the 17th are selected.

   Note: The Control key is used to select markers randomly. For example, you can
select the third marker and keeping the Control key pressed select the seventeenth marker. Design Association will highlight the third and the seventeenth marker. You can simultaneously select any number of markers randomly by using the Control key.

2. Click the Execute button.
   - The Execute All window appears showing the progress status. The Progress control progresses whenever a new action is executed.
   - For each selected marker, Design Association displays a message box asking you to place the component in the Concept HDL design.

3. Click the OK button to place the component in the Concept HDL design.

4. The Concept HDL window appears. Observe the pointer. It displays the component corresponding to the marker. You can move the pointer to any place in the Concept HDL window and click at that point.
   - The component corresponding to the marker is placed at the selected point.
   - If there are more components to be placed, Design Association displays a message window asking you to place the next component in the Concept HDL design. If you need to place more components, repeat steps 3 and 4.
   - Finally, the Design Association window appears informing you that multiple actions have been executed. The window also displays a Yes or No option that you can use to review the details of the actions.

5. If you want to stop Design Association from executing all the selected actions, click Stop.
   - If you click Stop while Design Association is executing an action, the current action is executed, but none of the remaining actions are not executed. You cannot undo the executed actions.
   - The Stop button changes to Cancel when all the selected actions have been executed.

6. Click Detail, which is a toggle button, on the Execute window if you want to view the details while all the actions are being executed.
   - The Execute window expands displaying all the details corresponding to each action as it gets executed. You can click Detail again to switch the Execute window back to the unexpanded state.

7. Save the design by using File - Save or File - Save As from the Concept HDL menu bar.
   - The design is saved.
Note: For an Add Instance action type, a new drawing page is added and all the instances are placed on that page.

Note: You can select multiple markers only with the following command menu items Action - Execute, Action - Mark As Completed, or Action - Clear Status.

Adding Locations, Nets, Instances, and Terminators

Adding a Location

Each marker is associated with a location, which represents the logical path name in the Concept HDL schematic where the marker will be executed. If the location is not attached to a marker or if you want to define a new location, you can add a location to that marker. To add a location to a marker,

1. Select a marker from the Markers list box.
   The Action - Add Location menu is enabled.
2. To add the location, choose Action - Add Location from the Design Association menu bar.
   The Add Location window appears with a selection box, which presents the location (the logical path name of the drawing) of the active page that you want to edit in the Concept HDL design.

Figure 6-7 Add Location Dialog Box

3. If the action displays the canonical path, you can edit the selection. Next, click OK on the Add Location window to add the specified location.
   The Design Association tool
❑ Adds the logical path name of the drawing in the active page in your Concept HDL design. If the location does not exist, the location is added as a new location in the current marker.

❑ Displays the new location below the parent marker as a magenta check box.

4. Select the marker corresponding to the new location or the default location from the Markers list box.

5. Choose Action - Execute from the Design Association menu bar.

   A message to place the component in your Concept HDL design appears in the status bar of the Design Association tool.

6. Zoom to the corresponding location in your Concept HDL design.

7. Place the component. After the action is executed, the magenta check box next to the new location is checked and the Action - Execute command is disabled.

Note: If you decide to add all the instances simultaneously using the Action - Execute command, Design Association adds a new page border. Before running the Action - Execute command, you must select Options - Set Up and indicate the drawing page size you need.

Adding a Net to a Pin

1. To add a net to a pin in the Concept HDL schematic, select the corresponding Add Pin Net marker in the Markers list box.

   Design Association opens the corresponding drawing page in your Concept HDL design and highlights the specified net.

2. Click Execute in the Design Association window or choose Action - Execute from the menu bar.

   The drawing page of the instance is edited, and the wire-segment pin is added to the instance port.

Note: If the pin-net connection cannot be made, the Design Association window appears with a warning message explaining why the task cannot be executed.

Note: The check box next to the tree node corresponding to the specific Add Pin Net marker changes based on the execution status of the action.

Adding an Instance

To add only one instance at a time,
1. To add an instance in the Concept HDL schematic, select the marker corresponding to the Add Instance action type.

Design Association automatically opens up the corresponding drawing page in the Concept HDL schematic where the instance is to be added. To change the location, add a new location and click that location.

2. Zoom to the section in the Concept HDL schematic where you want to add the instance.

3. Click Execute in the Design Association window or choose Action - Execute from the menu bar.

The instance to be added is attached to the pointer.

4. Place the instance in the section that you have zoomed into the Concept HDL schematic design.

After you place the instance on the corresponding drawing page location of the Concept HDL schematic, Design Association attaches the net stubs to the instance ports.

To add multiple instances simultaneously,

1. Select the markers that you want to add from the Markers list box by using the Shift or Control key.

2. Choose Options - Set Up from the menu bar and show the new drawing page size.

3. Choose the Action - Execute command. Design Association places the components on the Concept HDL schematic.

Note: The check box next to the tree node corresponding to the selected Add Instance markers changes depending on the execution status of the action.

Adding a Series Terminator

1. Select the marker corresponding to the Add Series Term action type.

Design Association automatically opens up the corresponding drawing page and highlights the pin where the series terminator is to be added.

2. Click Execute in the Design Association window or choose Action - Execute from the menu bar.

If you have not selected a point, the series terminator will be added at the same predefined distance from the driver pin in the Automatic mode. If you have selected the point where you want to add the series terminator, the series terminator is added there in the Interactive mode. To select a mode, use the Setup dialog box.
Adding a Shunt Terminator

1. Select the marker corresponding to the Add Shunt Term action type.

   Design Association automatically opens the corresponding drawing page and highlights the pin where the shunt terminator is to be added.

2. Click Execute in the Design Association window or choose Action - Execute from the menu bar.

   Depending on the mode selected in the Setup dialog box, the shunt terminator will either be added automatically or will be added at the point selected by you. If you have selected the Automatic mode, the Design Association tool selects the pattern of the shunt terminator that fits in the given place and the point where it can be added.

   If you have selected the Interactive mode, you can select different patterns of the shunt terminator by pressing the Control key and clicking the right mouse button. You can also select the point at which you want to add the given pattern of the shunt terminator.

Backannotating to Concept HDL

Loading the Feedback Files from the Current Packaged View Directory

1. To backannotate the changes to Concept HDL, choose Action - Backannotate from the Design Association menu bar.

   The Open dialog box appears showing an explorer view from which you can select the appropriate feedback files.

2. Browse to the packaged view directory or any other directory where you have the packaged files.

3. Select the format Data Files (*.dat) from the Files of type field.

4. Select the appropriate *.dat feedback files as described below:

   - Select the *view.dat files if you are backannotating from the Allegro layout tool.
   - Select the pstrprt.dat, pstxnet.dat, pstxprt.dat, and pstxref.dat files if you are backannotating from a third-party layout tool.

   The File name box is filled with the feedback file names you have selected.

5. Click Open in the Open dialog box to load the selected *.dat files for backannotation.
Changing Parts

You may want to change a part for only one instance at a time or for multiple instances simultaneously.

Changing Parts for a Single Instance

1. To change a part for a single instance, select the marker corresponding to the Change Part action type for that instance.
   
   Design Association automatically opens up the corresponding drawing page where the instance exists.

2. Click Execute in the Design Association window or choose Action - Execute from the Action menu bar.

   The property value of component_definition_property is changed or the property is deleted.

Changing Parts for Multiple Instances Simultaneously

1. To change parts for multiple instances, select the corresponding Change Part markers for each instance from the Markers list box using the Shift or Control key.

2. Choose Action - Execute All.

   The property value of component_definition_property corresponding to each selected marker is changed, or the property is deleted.

   **Note:** The status of the check box next to the tree node corresponding to the selected Change Part markers changes depending on the execution status of the action.

Deleting a Location

You can delete a selected location using the Action - Delete Location command. This command can be applied only to the locations specified by Add Instance action types. If you have any other action type, the Action - Delete Location command becomes unavailable for selection.

You cannot start the Action - Delete Location command if an Add Instance marker has only one location. The Design Association window appears with a warning that you cannot delete an instance that has only one location.

To delete a location,
1. Select the *Add Instance* marker corresponding to the location that you want to delete from the *Markers* list box.

   The *Action - Delete Location* command is enabled.

2. Choose *Action - Delete Location* from the Design Association tool menu bar.

   - The check box and the added location under the *Add Instance* parent marker are deleted.
   - The component corresponding to the marker in Concept HDL and its location are deleted from the design.

**Deleting a Net from a Pin**

To delete a net from a pin,

1. Select the *Delete Pin-Net* marker corresponding to the net that you want to delete.

   Design Association automatically opens the corresponding drawing page in the Concept HDL design highlighting the specific net that needs to be deleted.

2. Choose *Execute* or choose the *Action - Execute* menu command.

   - The drawing page containing the pin-net connection that needs to be deleted is edited.
   - The wire segment is deleted from the pin.

*Note:* If the action cannot be executed, you get a warning indicating that the pin on the instance is not connected to the net or the segment.

*Note:* The status of the check box next to the tree node corresponding to the selected *Delete Pin-Net* marker changes based on the execution status of the action.

**Deleting an Instance**

To delete an instance from the Concept HDL schematic,

1. Select the *Delete Instance* marker corresponding to the instance that you want to delete.

   Design Association automatically opens and highlights the instance that needs to be deleted from the corresponding drawing page of the Concept HDL schematic.

2. Choose *Execute* or click the *Action - Execute* menu command.
**Note:** If the instance cannot be deleted, the Design Association window appears with a warning message explaining why the instance cannot be deleted. Also, the check box next to the tree node corresponding to the specific **Delete Instance** action type changes depending on the execution status of the action.

### Replacing a Net on a Pin

To replace a pin-net connection, you can begin by expanding the marker. This is an optional step. Next, do the following steps:

1. **Select the Replace Pin-Net option in the Markers list box to define the action that you need to start.**
   
   The Design Association tool automatically opens up the corresponding drawing page in the Concept HDL schematic design in which the pin-net connection is to be replaced.

2. **Choose Action - Execute or choose the Action - Execute menu command.**
   
   The Design Association tool replaces the pin-net connection and the check box next to the marker changes to reflect the execution status of the action.

**Note:** If the pin-net connection cannot be replaced, the Design Association window appears with a warning message explaining why the action cannot be executed.

**Note:** It is possible to run multiple actions simultaneously.

### Replacing an Instance

Based on your requirements, you can select to replace only once instance or multiple instances simultaneously.

**Replacing Only One Instance at a Time**

1. **Select the Replace Instance marker corresponding to the instance that you want to replace. Design Association automatically opens up the corresponding drawing page where the instance is to be replaced.**

2. **Select the Interactive or Automatic option from Options - SetUp.**
   
   **Note:** In the Interactive mode, you can specify the location where you want to add the instance.

3. **Click Execute in the Design Association window or choose the Action - Execute menu command.**
The instance to be replaced is attached to the pointer.

4. Place the component in the section that you have zoomed into in your Concept HDL schematic design.

Design Association attaches the net stubs to the instance ports.

Replacing Multiple Instances Simultaneously

1. Select the Replace Instance markers corresponding to the instances that you want to replace by using the Shift or Control key.

2. Choose the Action - Execute All command.

Design Association replaces the components in the Concept HDL design.

Note: The check box next to the tree node corresponding to the selected Replace Instance markers changes based on the execution status of the action.

Filtering Action Types and Message Strings

1. Choose Options - Filter/Select from the Design Association window.

The Filter/Select Dialog Box appears.
2. Select the *Filter* radio button or the *Select* radio button in the *Mode* group.

3. Select *Filter* to indicate that you want to filter out all the markers in the *Markers* list box. Choose *Select* to show that you want to specify the markers to be executed.

4. Select the actions you need to start by clicking one or all options in the *Action Type* box.

   The *Markers* list box in the Design Association window lists only those action types that you have chosen.
5. To display the status of the action, select one or all options, Success, False, Failed, or Unexecutable, in the Execution group.

When an action is started, the check box to the left of the marker in the Markers list box in the Design Association dialog box changes in color based on the execution status of the action.

6. Enter an expression to filter the markers in the Short Message String field.

7. To exclude the specified regular expression that you typed in step 5 in the Short Message String field from the filter, click Exclude.

Note: If you select the Exclude check box, then only those short messages that do not match the specified regular expression are passed through this filter.

8. Click Select All or DeSelect All to select or clear all the options in the Action Type box or the Execution Status box.

9. Click OK to filter the markers.

All the markers matching your search criteria are displayed.

10. If you need to close the Filter/Select dialog box without filtering the markers, click Cancel.

Marking an Action as Completed

If you make a change without going through the Design Association tool, you can mark the action using the Mark as Completed command.

➤ Choose Action - Mark as Completed from the Design Association menu bar.

Note: You can select multiple selection of markers only with the following commands: Action - Execute, Action - Mark As Completed, and Action - Clear Status.

Opening and Saving the Markers File

Loading the Markers File

The Design Differences tool sends connectivity changes to the dessync.mkr file. Design Association uses this file as the input to apply the connectivity changes to the Concept HDL schematic and get the logical view in sync with the physical view. By default, Design Association generally starts loaded with the dessync.mkr file generated by Design Differences. If this does not happen, you can open and load the marker file using the following steps:
1. Choose File - Open from the Design Association menu bar.

   The Open Marker File dialog box appears with a list of marker files (*.mkr). Design Association opens the Open Marker File dialog box in the same directory where your project file (*.cpm) is located.

2. Use the Navigate button in the Look in box to navigate to the directory that contains the specific application directory whose marker file you need to load.

3. Double-click the application directory to open it.

4. Select the *.mkr file that has been generated by Design Differences from the application directory.

   The File field shows the marker filename, dessync.mkr.

5. Select the format marker Files (*.mkr), in the Files of type box.

6. Click Open in the Open Marker File dialog box to load the marker file dessync.mkr.

### Saving the Marker File

You must save the marker file before exiting Design Association to ensure that the execution status of an action is available for future Design Association sessions.

1. Choose File - Save from the Design Association menu bar.

   The current marker file is saved in the directory from where it was read, and a message box appears asking you to save your design in Concept HDL.

2. Choose File - Save Schematic from the Design Association menu bar to save the schematic design so that the marker file is in sync with your design.

**Note:** You can save the marker file with a different name by using the File - Save As command.

### Viewing Marker File Properties

1. Choose File - Properties from the Design Association menu bar. The Design Association window appears displaying the following:

   □ The full path to the current marker file

   **Note:** The path to the dessync.mkr file appears by default.

   □ The path to the current project file

2. Click OK to close the Properties window.
Miscellaneous Items

The following list covers miscellaneous terms that have been used in this guide.

Logical View

The set of files that Packager-XL uses to represent a schematic is called a logical view. The logical view shows information about the instances, nets, properties, and connectivity in a Concept HDL schematic database.

The logical view shows the following Packager-XL output files: pstxnet.dat, pstxprt.dat, and pstchip.dat.

Physical View

The set of files that Packager-XL uses to represent a layout is called a physical view. The physical view shows information about the instances, nets, properties, and connectivity in the Allegro layout database.

The physical view shows the following output files extracted by Allegro: pinview.dat, funcview.dat, netview.dat, and compview.dat.

Sample propflow.txt File

The propflow.txt file is used to define the properties that will be transferred between Concept and Allegro. A sample propflow.txt file is shown below:

OWNERT
0 - Undefined
1 - Component
2 - Instance
3 - Pin
4 - Net

Concept
0 - Not defined in concept
1 - Defined in concept

Allegro
0 - Not defined in allegro
1 - Defined in allegro

Transfer
0 - Not transferable between concept and allegro
1 - Transferable

WINNING_VALUE
0 - None
1 - Allegro
2 - Concept

TYPE
0 - Undefined
1 - String
2 - Integer

<table>
<thead>
<tr>
<th>PROPERTY_NAME</th>
<th>OWNER</th>
<th>CONCEPT</th>
<th>ALLEGRO</th>
<th>TRANSFER</th>
<th>WINNING_VALUE</th>
<th>TYPE</th>
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</thead>
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<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
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<tr>
<td>REFDES</td>
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<td>0</td>
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<tr>
<td>COMP_PARENT_PPT_PART</td>
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<tr>
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<td>0</td>
</tr>
<tr>
<td>COMP_NO_ROUTE</td>
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<td>1</td>
<td>1</td>
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<td>0</td>
</tr>
<tr>
<td>COMP_MAX_POWER</td>
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<td>0</td>
</tr>
<tr>
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<tr>
<td>NET_WEIGHT</td>
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<td>0</td>
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<td>0</td>
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</tr>
</tbody>
</table>

List of Properties Filtered from Packager Files

The predefined list of properties that are filtered out while reading packager output files is:

Pin Properties
NO_LOAD_CHECK
NO_IO_CHECK
ALLOW_CONNECT
PIN_GROUP

**Component Properties**

FAMILY
CLASS
PART_NAME
PHYS_DEF_PREFIX
PART_NUMBER
JEDEC_TYPE
DESCRIPTION
ALT_SYMBOLS
PARENT_PART_NAME
PARENT_PPT
PARENT_PPT_PART
BODY_NAME
POWER_PINS
SCH_MODIFIED_PART
TECH
DEFAULT_SIGNAL_MODEL

**Function Properties**

XY
PATH
Miscellaneous Items

DRAWING
PACK_TYPE
CDS_LIB
PRIM_FILE
PART_NUMBER
Index

A

action 146
  executing 159
  execution status 154
  marking as completed 172
action types 154
  Add Instance 155
  Add Pin Net 155
  Add Series Terminator 156
  Add Shunt Terminator 156
  Change Part 157
  Delete Instance 154
  Delete Pin Net 155
  Replace Instance 156
  Replace Pin Net 155
Add Instance action types 155
Add Pin Net action types 155
Add Series Terminator action types 156
Add Shunt Terminator action types 156

B

backannotating properties
  using the pxlba.txt file 94
board
  updating the changes in the schematic 79
BOM
  function 16
  generating 98

C

Change Part action types 157
comparing
  instance differences 137
  instance part differences 138
  instance property differences 138
  net differences 137
  net property differences 139
  pin property differences 139
  pin-net differences 138
  pin-swapping differences 140
  refdes differences 140
  section-swapping differences 140
  Concept-Allegro property flow 58

D

dehighlighting objects 132
Delete Instance action types 154
Delete Pin Net action types 155
design
  exporting 29
  importing
    Import Physical
    importing the design 32
  packaging 28
  querying a design using Design Differences 125
Design Association
  deleting instance 168
Detail window 168
  151
  exiting 148
  invoking 27
  overview 144
  replacing instance 169
Design Difference
  windows 114
Design Differences
  function 16, 17
  functions 108
  invoking 26, 108
  loading Allegro layout 124
  loading Concept-HDL schematic 124
  overview 104
  querying the design 125
  Toolbar 112
  user interface 112
  viewing errors 118
  viewing logical design 118
  viewing physical design 120
Design Synchronization
  invoking tools 26
  marker file 146
  overview 13
  summarizing 25
Design Synchronization and Packaging User Guide

toolset 14
dessync.mkr file 146
dialog box
Add Property 42
Add Query 127
BOM-HDL 99
Design Differences 32, 109, 110
Edit Query 130
Electrical Rules Check 100
Export Logic 87, 88, 89
Export Physical 30, 80
Filter Options for Differences 141
Filter/Select 171
Import From 66
Import Physical 33, 91, 92
Netlist Reports 102
Packager Setup 36
preview ECO on Allegro Board 134
Preview ECO on Schematic 148
Property Flow Setup 63, 96
Property Sheet 160
Query Design 126
Select Board File to Compare 125
Select Packaged View to Compare 124
View Results 103
difference view windows 114
difference views
regenerating 133
synchronizing 133
differences
comparing differences between logical and physical views 137
comparing instance differences 137
comparing instance part differences 138
comparing instance property differences 138
comparing net differences 137
comparing net property differences 139
comparing pin property differences 139
comparing pin-net differences 138
comparing pin-swapping differences 140
comparing refdes differences 140
comparing section-swapping differences 140
filtering 141
displaying a hierarchical tree in Design Association 158

E

Electrical Rule Check
function 16
Running 100
error messages 97
executing an action 159
exiting
Design Association 148
Export Physical
function 15
exporting the design 29

F

Feedback mode
running Packager-XL 86
feedback properties
changing in the layout 46
Filter Options for Differences dialog box 141
Filter/Select dialog box 171
filtering
differences 141
instance properties 142
instances 143
net properties 142
pin properties 142
filters 141
predefined list of filter properties 175
pre-defined properties filtered from packager files 174
Forward mode
running Packager-XL 79
Front-To-back flow
conventional 17
Front-to-back flow
Concept-Allegro property flow 58
Design Synchronization Flow 19
how Design Association fits in 144
where Packager-XL fits in 69
where VDD fits in 104

G

Genfeedformat
function 17
**Design Synchronization and Packaging User Guide**

**H**

hierarchical tree  
displaying  158  
highlighting objects  131

**I**

Import Physical  
function  15  
importing the design  32  
instance  
deleting  168  
replacing  169  
instance properties  
filtering  142  
instances  
filtering  143  
invoking  

- Design Association from Concept-HDL  147  
- Design Differences from Concept-HDL  147

**L**

loading  
Allegro layout in Design Differences  124  
Concept-HDL schematic in Design Differences  124  
marker file  172  
logical design view window  116

**M**

marker file  
loading  172  
saving  173  
viewing properties  173  
markers  146  

displaying  153  
expanding  158  
Markers List Box  151, 153  

modes  
Feedback  86  
Forward  79

Packager-XL operation modes  70

**N**

net properties  
filtering  142  
netlist parameters  
changing  51  
Netlist Reports  
function  16  
Netrev  
function  17

**O**

objects  

dehighlighting  132  
highlighting  131  
highlighting and dehighlighting  131  

opening  
Property Flow Setup dialog box  60  
overview  
Concept-Allegro property flow  58  
Design Association  144  
Design Synchronization  13  
packaging your design  68  

resolving design differences  104

**P**

packager output  
changing  48  
Packager Setup  
changing properties  39  
function  15  
invoking  27  
Packager Setup dialog box  35  
From Layout tab  37  
Layout tab  38  
Properties tab  37  
Report tab  38  
seeding the default Packager properties  67  
State File tab  37  
Subdesign tab  38  
Packager Setup options  
defining  28  
packager setup options
Design Synchronization and Packaging User Guide

changing 54
Packager Utilities
  introduction 15
  invoking 27
Packager utilities
  generating BOM 98
  running Electrical Rule Check 100
  using 97
  viewing any files 103
Packager-XL
  directives 78
  exit status 97
  Feedback mode 74
  Forward mode 71
  inputs in Forward mode 72
  inputs to Feedback mode 76
  modes 70
  outputs from Forward mode 73
  prerequisites for running 79
  properties 78
  running in Feedback mode 86
  running in Forward mode 79
  physical design view window 116
  pin properties
    filtering 142
  Preview ECO on Schematic dialog box 148
  properties
    adding and deleting 41
    filtered from packager files 174
  property flow
    from Concept-HDL to Allegro 59
    setting 63
  Property Flow Setup dialog box
    opening 60
    seeding default pxlba.txt file
      properties 66
  Property Sheet dialog box 160
  propflow.txt file 174
  pxlba.txt file
    controlling backannotation of
      properties 94
    displaying 95

Q
querying the design 125

R
reference designators
  changing 51
  Replace Instance action types 156
  Replace Pin Net action types 155
  replacing
    instance 169

S
saving
  marker file 173
  schematic
    comparing with the layout 31
    synchronizing for ECO changes 135
    updating the changes in the board 86
  Setup Window 160
  state file 42
    changing the packaging information 43
    synchronizing
      schematic for ECO changes 135

T
tools
  BOM 16
  Design Differences 16
  Electrical Rule Check 16
  Export Physical 15
  Genfeedformat 17
  Import Physical 15
  Netlist Reports 16
  Netrev 17
  Packager Setup 15
  Packager Utilities 15

V
view
  logical 174
  physical 174
viewing
  Design Differences errors 118
  differences in the schematic and the
Design Synchronization and Packaging User Guide

layout in a Text Editor  121
hierarchical trees  122
logical design  118
physical design  120
viewing any files  103
Visual Design Differences
function  16

W

window
Design Difference  114
logical design view  116
physical design view  116
rearranging Design Difference
windows  117
Design Synchronization and Packaging User Guide