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Introduction to the Tutorial

Purpose

The Design Synchronization tutorial describes how to keep schematics and boards in sync using the Design Synchronization toolset. The tutorial focuses on the following set of procedures:

- Annotating the connectivity changes made in the board back to the schematic
- Annotating the property changes made in the board back to the schematic
- Synchronizing the schematics and boards using the Design Synchronization toolset

Audience

This tutorial is designed for first time users of the Design Synchronization toolset. If you are a schematic or board designer, you will find that you often require to synchronize the schematic and the board. This requirement would come if you make property or connectivity changes to the schematic or the board after initial packaging. The use of the Design Synchronization toolset helps you to keep the schematic and the board in sync.

Prerequisites

It is assumed that you are familiar with Concept HDL and Allegro. This document will not discuss the details of taking a design from the schematic to the board as it is assumed that you are familiar in working with these tools.

Note: To learn about Concept HDL or Allegro, see Concept HDL User Guide and Allegro/APD Design Guide in CDSDoc.
Design Synchronization Toolset

Design Synchronization tools are used to compare schematics and boards and provide categorized output. They also provide the facility to update changes either way, from a board to the schematic and from a schematic to the board.

The Design Synchronization toolset consists of:

- Design Differences
- Design Association
- Packager-XL
- Netrev
- Genfeedformat

The Design Differences and Design Association tools are the focus of this tutorial.

**Design Differences** - This tool compares a schematic and a board, and presents the differences in connectivity, nets, and parts, net properties, pin properties, and component properties, and so on. Design Differences allows you to control the updating of the schematic or the board. Design Differences is also referred to as Visual Design Differences or VDD.

**Design Association** - Design Differences dumps the connectivity changes between the schematic and the board in a file named `dessync.mkr`. Design Association reads these changes and allows you to update the schematic in a controlled manner.

**Packager-XL** - Packager-XL is the interface between the logical design (schematic) and the physical layout (board) for the Cadence Board Design Solution. It has two modes of operation:

- In the Forward mode, Packager-XL translates a logical design entered in Concept HDL into a physical design ready for layout by Allegro.
- In the Feedback mode, Packager-XL receives changes made in Allegro and incorporates the property/swapping changes back to the logical design.

**Netrev** - Netrev loads the Packager output into a database for physical layout, which can be operated on by Allegro or SPECCTRAQuest.

**Genfeedformat** - Genfeedformat extracts connectivity and property information from the board into view files that are used by Design Differences and Packager-XL (in the Feedback mode).
Overview

Design Synchronization tools are used to compare a schematics and a board, and synchronize any changes in them. The primary need for synchronization is caused by changes that occur either in the board or in the schematic after the initial transfer of packaged information to the board.

The changes that occur in the board after the initial transfer of packaged information from the schematic are of the following four types:

1. Component changes
   You may add new components in the design to handle signal integrity and electromagnetic compatibility problems. These components may include termination resistors, series or shunt buffers, and bypass capacitors.

2. Connectivity changes
   You may make connectivity changes to facilitate routing after the initial placement of components. Connectivity changes may be caused by pin swaps, section swaps, and reference designator (refdes) swaps.

3. Reference designator changes
   You may change reference designators to debug board problems.

4. Property changes
   You may modify certain components in the board. These modifications will cause property changes.

Besides the changes in the board after the initial transfer of packaged information from the schematic, certain changes such as Engineering Change Order (ECO) are also made in the schematic. The need for Design Synchronization toolset arises from the need to synchronize the above mentioned differences between the schematic and the board.

This tutorial will cover the Design Differences and Design Association tools. You will use these tools to synchronize a given schematic and board, which are part of the database available with the tutorial.

**Note:** For more information about different Design Synchronization tools and how they fit in the Front-to-back flow for PCB system design, see the Cadence document *Design Synchronization and Packaging User Guide* in CDSDoc.

The tutorial consists of eight chapters. Each chapter deals with a particular type of difference between the board and the schematic. The chapters are named after the causes behind the differences between the schematic and the board. The names of different chapters are:
Tutorial Structure

This section explains the installation and structure of the tutorial. Each chapter includes additional information about specific features of the tools. After completing this tutorial, you will be able to use the tools fluently in their design process.

Installing the tutorial

Windows NT

Unzip the dessync_db.zip file located in the <your_inst_dir>share/fet/examples/designsync, and extract it to an empty directory, say ds_demos. On extracting the dessync_db.zip file, you will find 8 sub-directories are created under the ds_demos directory. Each of these sub-directory has a design relevant to each section of the tutorial.

UNIX

Uncompress and untar the file dessync_db.t.Z, and extract the information to an empty directory, ds_demos. This directory serves as the demo directory for this tutorial.

Setting the CDS_INST_DIR variable

Ensure that the CDS_INST_DIR variable is set to point to the directory where you install PCB tools.
Structure of the Demo Database

The ds_demos database consists of 8 directories, each of which contains a design with all the required views. The directory contains one schematic and one or more boards. The project directory is hdli for all the sections. The design directory is called fx, while the project file is atm.cpm.

The procedure in each chapter is as follows:

1. Invoke Project Manager and load atm.cpm.
2. Open the schematic file in Concept HDL.
3. Open the board file sync.brd using Allegro. There are other boards present, which are not in sync with the schematic.
4. Use Design Differences to verify that the schematic and the sync.brd file are in sync.
5. Use Design Differences to view the differences between the board and the schematic.
6. Update the Concept HDL schematic.
7. Run backannotate in Concept HDL and view the changes.

Note: In Release 14.2, you can directly backannotate the schematic from Export Physical and Import Physical.

8. Save and package the schematic.
9. Use Design Differences to ensure that the new schematic and difference board are in sync.

Note: Remove the fx directory, and copy fx.orig to fx in the project directory to reuse the tutorial database.
Handling Pin Swaps

Objective

To become familiar with Visual Design Differences (VDD) and to see how pin swap information is displayed in VDD. You will use this information to update the schematic.

At the end of this chapter, you will be able to:

- Invoke Design Differences from Concept HDL.
- Use Design Differences to view the differences caused by pin swaps in the board.
- Synchronize the schematic with the pin swaps made in the board.

Starting PSD Tools

To understand the working of Design Differences, you need to be aware about Project Manager, Concept HDL, and Allegro. These are the PSD tools in the Front-to-back flow that call Design Differences to identify differences between the schematic and the board.

Task Overview

You will open the atm.cpm file in the ds_demos/pinswap/hdli directory in Project Manager, and view the schematic in Concept HDL and the board in Allegro.

Steps

1. Launch Project Manager by typing the following command in the command window:
   
   ```plaintext
   projmgr &
   ```

   **Note:** You may double-click the projmgr.exe file in Windows-based systems to launch Project Manager.

2. From the *File* menu, Select *Open*. 
The Open Project file browser is displayed. You can select the name of the project file here.

3. Load the `atm.cpm` file located in the `ds_demos/pinswap/hdli` directory.
   
   Notice that the Project Manager's Title Bar displays the title `atm.cpm`.

4. Click on the Design Entry icon in Project Manager to open the schematic in Concept HDL.
   
   Concept HDL opens the `atm.cpm` project and displays the schematic.

5. Click on the Layout button in Project Manager to launch Allegro.
   
   Allegro opens the `atm.cpm` project and displays the board.


**Starting Design Differences**

**Task Overview**

You will start Design Difference from Concept HDL and load the `sync.brd` board file. This will enable you to view the differences between the schematic and the board.

**Steps**

1. Select Tools > Design Differences in Concept HDL to start Design Differences.

   Concept HDL displays a message box (see Figure 1-1 on page 14) informing that the design needs to be expanded before you can run Design Differences. Design expansion is a necessary step for the cross-probe utility in Design Differences to highlight signals in the schematic. You need to click Yes to proceed with design expansion or click No to stop launching Design Differences.
2. Click Yes to display the Design Difference window.

   The Design Differences window appears with the title “Design Differences - atm”.

3. Click on the *Browse* button.

   A list box comes up with the boards that can be compared with the schematic.

4. Select *sync.brd* from the list box.

   **Note:** The *Update board view before compare* check box needs to be selected for the *Browse* button to be enabled.

   When the *Update board view before compare* check box is selected, Design Differences compares the packager feedback files (generated by running *genfeedformat* on the board) with the packager files and generates feedback files for
the selected board. If this check box is not selected, Design Differences will use the view files already present to compare differences.

Similarly if you have selected the *Update package view before compare* check box, Design Differences will package the saved schematic (by calling Export Physical). The *Options* button will bring up the packaging options form. Do not select this option because the schematic has not changed after it was packaged initially.

5. Click *OK* in the Design Differences dialog box.

The Progress Window appears.

**Figure 1-3 Progress Window**

The progress window disappears as soon as the views are updated.

The Design Differences window is displayed, and the following message box appears stating that no differences exist between the schematic and the board.
6. Click **OK** to close the message box.

   The rest of the Design Differences window is now activated for other operations. The message log window is left open.

### Viewing Pin Swap Design Differences

#### Task Overview

You have verified that the schematic is in sync with the **sync.brd** board file. You can now compare the schematic with a board in which a pin swap has occurred using Design Differences. First, you will view the differences manually, and then, see how the differences show up in the Design Differences window.

#### Steps

1. Select **File > Open** in Allegro and load the **pin_swapped.brd** board file.

   Notice the two ratsnest lines in red. One line connects the pins **U7.7** and **U8.5**, and the other line connects pins **U3.4** and **U8.4**.

2. Select **File > Edit Hierarchy > Descend** in the Concept HDL window. Descend into the **CNTR10** block in the top-level schematic by clicking on the **Descend** button on the toolbar below the **group** command. Locate the OR gates in **U8** in the lower left corner of the schematic. You can use the command **find u8** in the Concept HDL console window.
to find U8 and use next to get to the right pins. Notice that U8.4 is connected to U7.7, and U8.5 is connected to U3.4.

<table>
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<th>SCHEMATIC</th>
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<tr>
<td>U3.4-U8.5</td>
<td>U3.4-U8.4</td>
</tr>
<tr>
<td>U7.7-U8.4</td>
<td>U7.7-U8.5</td>
</tr>
</tbody>
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You will next view the same information in the Design Differences window.


The Select Board File dialog box appears.

Figure 1-5 Select Board File Dialog Box

4. Select the pin_swapped.brd file from the list box.

Design Differences loads the board and a message box displays the message “Reload Allegro Board has successfully completed!”.

5. Click OK to proceed.

The Design Differences window now shows the differences. Notice the two windows within the Design Differences main window. One of them is the Message log window and the other shows the pin swapping information.

6. If the Pin Swapping window is not in front, select Difference > Pin Swapping to bring it to the front.
The Pin Swapping differences window shows the differences in the \texttt{CDS\_PN} property, which has the physical pin number information. The first line informs that the \texttt{Refdes U8, part 74F32-BASE, section 2, schematic instance pin b<0> is mapped to the pin number 5 in the schematic but maps to the pin number 4 on the board.}

\textbf{Figure 1-6 Pin Swapping Window}

\begin{table}
\begin{tabular}{|l|l|l|l|l|l|l|l|}
\hline
Property & Name & Schematic Value & Board Value & Pin & Pin # & Section # & RefDes & Part \\
\hline
CDG\_PN & 5 & 4 & B... & 2 & U6 & 74F32-EASE & @
\hline
CDS\_PN & 4 & 5 & A... & 2 & U8 & 74F32-EASE & @
\hline
\end{tabular}
\end{table}

\textbf{Synchronizing the Schematic and the Board With Pin Swap Changes}

\textbf{Task Overview}

Update the schematic with the difference information and verify that the schematic is in sync with the \texttt{pin\_swapped.brd} board.

\textbf{Steps}

1. Select \textit{Sync > Update Concept Schematic} from the Design Differences window.

   The \textit{Preview ECO on Schematic Dialog Box} figure on page 19 appears. This dialog box summarizes the changes that will be carried out on the schematic to bring it in sync with the board.
You will now Launch Packager-XL in the feedback mode to update the pin swap information back to the packager files. Look at the changes in the Property Changes List. These changes will be carried out by Packager-XL when it runs in the Feedback mode.

2. **Click OK** to update the schematic

The Message log in the Design Differences window is updated and the Import Physical dialog box is displayed. See Figure 1-8 on page 20. Notice that you are not allowed to generate the feedback files. There is an option to backannotate the schematic. Do not select this option as then you would not be able to see the differences between the schematic and the board.
Design Synchronization Tutorial
Handling Pin Swaps

Figure 1-8 Import Physical Dialog Box: For Design Differences

3. Click OK.
   A Progress Window appears mentioning that design is netlisted and being fed back. Finally a message box appears asking whether you want to see Packager results.

Figure 1-9 Design Sync Message Box

4. Click No.
The Control is passed back to Design Differences, which displays a message that schematic has successfully loaded.

Figure 1-10 Design Differences Message Box

5. Click OK.

Design Differences compares the board and the schematic information. It has detected no differences.

Figure 1-11 Design Differences Message Box

6. Click OK to close the message box.

7. Select *Tools > Back Annotate* in the Concept HDL window to update the Concept HDL schematic with the changes in the packager files using the `pstback.dat` file.
Notice that the Package Backannotation check box is selected and the `pstback.dat` file in the packaged view is selected for backannotation. You also have an option to backannotate electrical constraints. Since the current design does not have any electrical constraints, we will not update them.

8. Click **OK**.

Concept HDL schematic is updated with the latest property information from the board. You can locate the U8 component in Concept HDL and see its pin configuration. You will find that the pins have swapped. The new pin connection for the U8 component is same as in Allegro board.

<table>
<thead>
<tr>
<th>SCHEMATIC</th>
<th>BOARD</th>
</tr>
</thead>
<tbody>
<tr>
<td>U3.4 - U8.4</td>
<td>U3.4 - U8.4</td>
</tr>
<tr>
<td>U7.7 - U8.5</td>
<td>U7.7 - U8.5</td>
</tr>
</tbody>
</table>

9. Select **File > Exit** in Design Differences, Allegro, Concept HDL, and Project Manager. Do not save any changes.
Handling Section Swaps

Objective

To see how section swap information is displayed in Design Differences and how it is updated in the schematic.

At the end of this chapter, you will be able to:

- Invoke Design Differences from Project Manager.
- Use Design Differences to view the differences caused by section swaps in the board.
- Synchronize the schematic with the section swaps made in the board.

Launching Design Differences from Project Manager

Task Overview

You will open the atm.cpm file in the ds_demos/section_swap/hdli directory in Project Manager, and view the schematic in Concept HDL and the board in Allegro.

Steps

1. Invoke Project Manager by typing the following command in the command window:
   
   `projmgr &`

   **Note:** You may double-click the `projmgr.exe` file in Windows-based systems to launch Project Manager.

2. Select *File > Open*.

   The Open Project file browser is displayed. You can select the name of the project file here.
3. Load the `atm.cpm` file located in the `ds_demos/section_swap/hdli` directory.

   Notice that the Project Manager's Title Bar displays the title `atm.cpm`.

4. Click on the `Design Entry` icon in Project Manager to open the schematic in Concept HDL.

   Concept HDL opens the `atm.cpm` project and displays the schematic.

5. Click on the `Design Sync` icon in the Project Manager Flow, and select `Design Differences` from the pop-up menu.

   The Design Differences dialog box is displayed. Notice that the `Update board view before compare` check box is selected.

6. Click on the `Browse` button, and select the `sync.brd` file.

7. Ensure that the `Update package view before compare` check box is not selected.

8. Click `OK` to launch Design Differences.

   The Progress window appears. You may click on the `Details` button in this window to see the progress log.

Figure 2-1 Progress Window
The Progress window disappears as soon as the views are updated. The Design Differences window is displayed, and a message box appears stating that no differences exist between the schematic and the board.

**Viewing Section Swap Differences in Design Differences**

**Task Overview**

Load the `section_swapped.brd` board file in Design Differences to view the section swap differences between the schematic and the board.

**Steps**

1. Select `File > Open` in Allegro, and load the `section_swapped.brd` board file.
   Notice the two pink ratsnest lines, which show the section swap that has been made.

2. Select `File > Load Allegro Board` in Design Differences, and select `section_swapped.brd` in the Select Board File to Compare dialog box. You can select the board by double-clicking on it.
   A message box appears with the message “Reload Allegro Board has successfully completed!”

3. Click `OK` to proceed.
   You see some messages scrolling in the “Message Log Window” within Design Differences. One more windows comes up. This window contains the section swap information.

4. Scroll up to the top of the Message log window.
   See the messages that appear. Note that the date and time of the loading of the view are mentioned at the top.

5. Press `Ctrl+F6` to go to the next window.
   The Section Swapping window becomes active.
Design Synchronization Tutorial
Handling Section Swaps

Figure 2-2 Section Swapping Window

<table>
<thead>
<tr>
<th>Property</th>
<th>Name</th>
<th>Schematic Value</th>
<th>Board Value</th>
<th>Section #</th>
<th>RefDes</th>
<th>Part</th>
<th>Where</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>CD...</td>
<td>6</td>
<td>4</td>
<td></td>
<td>U3</td>
<td>74...</td>
<td>@fx.a</td>
</tr>
<tr>
<td></td>
<td>CD...</td>
<td>4</td>
<td>6</td>
<td></td>
<td>U3</td>
<td>74...</td>
<td>@fx.a</td>
</tr>
</tbody>
</table>

The title reads “Section Swapping: atm(sch_1) vs. atm(section_swapped.brd)”. This window displays the top-level schematic and the name of the board being compared. Look at the columns.

The Name column represents the name of the property that is different between the board and the schematic. Notice that the name is incomplete and is represented by “CD...”.

6. Expand the Name column. For this, take the cursor to the divider line between Name and Schematic Value. The cursor shape will change. Click on the line and drag the mouse to extend the column to the required size.

The enlarged window with the expanded Name column is shown below.

Figure 2-3 Section Swapping Window: Fields Adjusted

Notice that the property name is CDS_SEC. You can adjust the size of any field in Design Differences window. Also notice that section 4 on U3 has been swapped with section 6 on the same IC.
Viewing Simultaneous Section and Pin Swap Changes in the Board

Task Overview

Load the section_swapped2.brd board file in Design Differences to view the section swap and pin swap differences between the schematic and the board.

Steps

1. Select File > Open in the Allegro window.
   You may get a message box asking whether you want to save the section_swapped.brd file. If you get the message, click No.

2. Load the section_swapped2.brd board, which is created by swapping section 1 with section 3 on U8 on sync.brd.
   Note: The highlighted nets are connected between U8.1 and U9.6 and between U8.2 and U8.8.

3. Select File > Load Allegro Board in Design Differences, and select the section_swapped2.brd board file in the Select Board File to Compare dialog box.
   A message box appears with the message “Reload Allegro Board has successfully completed!”

4. Click OK to proceed.
   You see some messages scrolling in the “Message Log Window” within Design Differences. Two more windows display. One window contains the section swap information and the other window contains the pin swap information.

5. Select Window > Horizontal Tile to arrange the three subwindows one below the other. This will help you see both section swaps and pin swap information simultaneously.
   The Pin Swapping window is shown below:
Design Synchronization Tutorial
Handling Section Swaps

Figure 2-4 Pin Swapping Window

Notice that pin 10 on the schematic is connected to pin 1 on the board, and pin 9 on the schematic is connected to pin 2 on the board.

Synchronizing the Schematic and the Board With Section Swap Changes

Task Overview

You will now update the schematic and ensure that the schematic and board are in sync after the update.

Steps

1. Select **Sync > Update Concept Schematic** from the Design Differences window.
   
   The Preview ECO on Schematic dialog box is displayed. The **Property Changes List** displays section swaps and pin swaps. Notice that the **Click Ok button to launch Packager to backannotate property changes to the schematic check box is selected**.

2. Click **OK** to update the schematic.
   
   The Message log in the Design Differences window is updated and the Import Physical dialog box is displayed.

3. Click **OK**.
   
   A Progress Window appears mentioning that design is netlisted and being fed back. Finally a message box appears asking whether you want to see Packager results.

4. Click **No**.
   
   The Control is passed back to Design Differences, which displays a message that schematic has successfully loaded.
5. Click OK.

   Packager-XL runs in the feedback mode and updates the packager files. Changes are also made to the Concept HDL schematic. A message box appears displaying the message that the schematic and the section_swapped2.brd board file are in sync.

6. Click OK to close the message box.

7. Select File > Exit in Design Differences, Allegro, Concept, and Project Manager. Do not save any changes.
Handling Section Swaps Between Components

Objective

To see how section swap between components is displayed in Design Differences and how it is updated in the schematic.

At the end of this chapter, you will be able to:

- Invoke Design Differences from the command line.
- Use Design Differences to view the differences caused by section swaps between components in the board.
- Synchronize the schematic with the section swaps between components made in the board.
- Cross-probe differences between schematic and Design Differences.

Setting Up and Launching Design Differences

Task Overview

You will open the atm.cpm file in the ds_demos/component_swap/hdli directory in Project Manager, and view the schematic in Concept HDL and the board in Allegro.

Steps

1. Invoke Project Manager by typing the following command in the command window:
   `projmgr &`
   
   **Note:** You may double-click the `projmgr.exe` file in Windows-based systems to
Design Synchronization Tutorial
Handling Section Swaps Between Components

launch Project Manager.

2. Select File > Open.

   The Open Project file browser is displayed. You can select the name of the project file here.

3. Load the atm.cpm file located in the ds_demos/component_swap/hdli directory.

4. Click on the Design Entry icon in Project Manager to open the schematic in Concept HDL.

   Concept HDL opens the atm.cpm project and displays the schematic.

5. Select Tools > Expand Design in the Concept HDL window to ensure that the design is expanded.

6. Select Tools > Design Differences in the Concept HDL window to launch Design Differences.

   The Design Differences dialog box is displayed. Notice that the Update board view before compare check box is selected.

   Note: You may launch Design Differences directly from the command-line prompt by using the vdd& command in UNIX.

7. Click on the Browse button, select the sync.brd file in the Select Board File dialog box, and click OK to close the dialog box.

8. Click OK to launch Design Differences.

   The progress control window appears displaying the message that views are being updated. When the views are updated, the progress control window disappears and the Design Differences window appears displaying the message that no differences exist between the schematic and the board.

9. Click OK to close the message box.

Viewing Differences Caused by Section Swap Between Components

Task Overview

You have verified that the schematic is in sync with the sync.brd board. You can now compare the schematic with a board in which a section swap has occurred between two
components using Design Differences. The `section_swapped_u3-u10.brd` board available in the physical directory under the atm design includes a section swap between the U3 and U10 components.

First, you will view the differences manually in Allegro, and then verify the differences in Design Differences. Project Manager is loaded with the `ds_demos/component_swap/hdli/atm` project.

**Steps**

1. Click on the *Layout* button in Project Manager to launch Allegro.
   
   Allegro opens the *atm.cpm* project and displays the board.

2. Select *File > Open* in Allegro, and load the `section_swapped_u3-u10.brd` board file.
   
   Notice the pink ratsnest lines, which show the section swap that has been made.

3. Select *File > Load Allegro Board* in Design Differences, and select `section_swapped_u3-u10.brd` in the Select Board File to Compare dialog box and click *OK*.
   
   A message box appears with the message “Reload Allegro Board has successfully completed!”

4. Click *OK* to proceed.
   
   You see some messages scrolling in the “Message Log Window” within Design Differences. Two more windows, RefDes Difference and Section Swapping, appear.

   The Section Swapping window is active. This window displays the CDS_SEC property in the schematic and the board is swapped. As a result, the RefDes U3 has value 1 in schematic and 6 in board while the RefDes U10 has value 6 in schematic and 1 in board.

**Figure 3-1 Section Swapping Window**

<table>
<thead>
<tr>
<th>Property</th>
<th>Name</th>
<th>Schematic Value</th>
<th>Board Value</th>
<th>Section #</th>
<th>RefDes</th>
<th>Part</th>
<th>Wh</th>
</tr>
</thead>
<tbody>
<tr>
<td>CDS_SEC</td>
<td>1</td>
<td>5</td>
<td>6</td>
<td>U3</td>
<td>74F04-BASE @F2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CDS_SEC</td>
<td>6</td>
<td>1</td>
<td>6</td>
<td>U10</td>
<td>74F04-BASE @F2</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

5. Press *Ctrl+F6* to go to the next window.
The RefDes Difference window becomes active. Notice that the CDS_LOCATION property in the schematic and the board is swapped. The section 1 of U10 has moved to U3 and the section 6 of U3 has moved to U10.

Figure 3-2  RefDes Difference Window

<table>
<thead>
<tr>
<th>Property</th>
<th>Name</th>
<th>Schematic Value</th>
<th>Board Value</th>
<th>Section</th>
<th>RefDes</th>
<th>Part</th>
<th>Who</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>CDS_LOCATION</td>
<td>U10</td>
<td>J3</td>
<td>6</td>
<td></td>
<td>74F04-BASE</td>
<td>@fx</td>
</tr>
<tr>
<td></td>
<td>CDS_LOCATION</td>
<td>U3</td>
<td>J10</td>
<td>1</td>
<td></td>
<td>74F04-BASE</td>
<td>@fx</td>
</tr>
</tbody>
</table>

Tip
To close any difference window, click on the Close button at the top left corner of the window. You may open any difference window by selecting it from the Difference menu. For example, you may close the RefDes Difference window by clicking on its close window, and open it again by selecting Difference > Refdes Swapping.

Cross-probing Between the Schematic and Design Differences

Task Overview
You will now cross-probe difference between the schematics and Design Differences. This helps you get a much better feel of what is going to happen in the schematic upon synchronization of differences.

Steps
1. Ensure that both Concept HDL and Design Differences are visible on the screen. Bring the Refdes Difference window in Design Differences to the front, and select the first line with the Schematic Value U10.
2. Select Display > Highlight Source in Design Differences to highlight an instance in the schematic.
   This highlights U10 as in Source Highlighted in Concept HDL figure on page 36.
3. Select Display > Dehighlight Source in Design Differences to dehighlight the highlighted instance.

   The highlight from the section 6 of U10 is removed.

4. Bring the Section Swapping window to the front and select the first line reading CDS_SEC 1. Click on the Highlight toolbutton to highlight the selection in the schematic.

5. Click on the right mouse button and a menu comes up. Select Dehighlight Source with the left mouse button to remove the highlight from the selection.

   **Note:** You may select a row in any Design Differences window and double-click on it. This will cause the selection corresponding to the difference to be highlighted in Concept HDL.

---

**Updating the Schematic with the Changes in the Board**

**Task Overview**

You will now update the schematic and ensure that the schematic and board are in sync after the update. Update the schematic by using the Backannotate command in Concept HDL.

**Steps**

1. Select Sync > Update Concept Schematic in Design Differences.
The Preview ECO on Schematic dialog box appears. The Property Changes List displays the list of changes in properties.

**Figure 3-4 Preview ECO on Schematic Dialog Box**

2. Click OK to update the schematic.

   The Message log in the Design Differences window is updated and the Import Physical dialog box is displayed.

3. Click OK.

   A Progress Window appears mentioning that design is netlisted and being fed back. Finally a message box appears asking whether you want to see Packager results.

4. Click No.
The Control is passed back to Design Differences, which displays a message that schematic has successfully loaded.

5. Click OK.

Packager-XL runs in the feedback mode and updates the packager files. Changes are also made to the Concept HDL schematic. A message box appears displaying the message that the schematic and the `section_swapped_u3-u10.brd` board file are in sync.

6. Click OK to close the message box.

7. Select *Tools > Back Annotate* in the Concept HDL window to update the Concept HDL schematic with the changes in the packager files using the `pstback.dat` file.

   Notice that the *Package Backannotation* check box is selected and the `pstback.dat` file in the packaged view is selected for back annotation. You also have an option to back annotate electrical constraints. Since the current design does not have any electrical constraints, we will not update them.

8. Click OK.

   Concept HDL schematic is updated with the latest property information from the board.

   The design differences are updated in Concept HDL. You may confirm these changes manually.

   However, a cleaner way to find whether no design differences exist between the schematic and the board is to use Design Differences. Since the schematic has changed, you need to repackage it before you use Design Differences.

9. Select *File > Export Physical* from Concept HDL to repackage the schematic.

   The Export Physical dialog box appears.

10. Select the *Package Design* check box and de-select the *Update Allegro Board* check box, and click OK.

   The design is packaged and a message box appears asking whether you want to review the log files.

11. Select No.


   A message box appears stating that the schematic and the `section_swapped_u3-u10.brd` board file are in sync.

13. Click OK.
14. Select *File > Exit* in Design Differences, Allegro, Project Manager, and Concept HDL. Do not save any changes.
Synchronizing Net Properties
Differences

Objective
To see how net property differences are displayed in Design Differences and how they are updated in the schematic.

At the end of this chapter, you will be able to:

■ Use Design Differences to view the differences caused by changes in net properties.
■ Decide which property difference to view and which property difference to ignore in Design Differences.
■ Backannotate property changes to the schematic using Design Differences.

Viewing Net Property Differences

Task Overview
You will open the atm.cpm file in the ds_demos/net_properties/hdli directory in Project Manager, and view the schematic in Concept HDL and the board in Allegro. First, compare the differences between the schematic and the sync.brd file. Next, compare the differences between the schematic and the route_priority.brd file.

Steps
1. Launch Project Manager by typing the following command in the command window:
   ```
   projmgr &
   ```
   Note: You may double-click the projmgr.exe file in Windows-based systems to launch Project Manager.
2. Select *File > Open.*
   The Open Project file browser is displayed. You can select the name of the project file here.

3. Load the *atm.cpm* file located in the *ds_demos/net_properties/hdli* directory.

4. Click on the *Design Entry* icon in Project Manager to open the schematic in Concept HDL.
   Concept HDL opens the *atm.cpm* project and displays the schematic.

5. Select *Tools > Design Differences* in Concept HDL.
   A message box stating that Design Differences requires you to expand the design appears.

6. Click *Yes.*
   The Design Differences dialog box is displayed.

7. Click on the *Browse* button, select the *sync.brd* file in the Select Board File dialog box, and click *OK* to close the dialog box.

8. Click *OK* to launch Design Differences.
   A message box stating that no differences exist between the schematic and the board (*sync.brd*) appears.

9. Click *OK* to close the message box.
   You have compared that differences do not exist between the schematic and the board (*sync.brd*) file. You will now compare whether differences exist between the schematic and the board (*route_priority.brd*) file.

10. Click on the *Layout* button in Project Manager to launch Allegro.

11. Select *File > Open* in Allegro and load the board *route_priority.brd* file.

12. Select *Display > Property* in Allegro.
   The *Show Property Dialog Box* figure on page 42 appears.
13. Select the property **ROUTE_PRIORITY**, and click on the *Show Val* button.

   A window appears showing that the **CLK** net has the **ROUTE_PRIORITY** property attached to it.

14. Verify that the **CLK** net in Concept HDL does not have the property **ROUTE_PRIORITY** attached to it.
Tip

You may use the Global Find dialog box to search for the CLK net and then check its properties.

15. Select File > Load Allegro Board in Design Differences, and load the route_priority.brd board file in the Select Board File to Compare dialog box, and click OK.

A message box appears with the message “Reload Allegro Board has successfully completed!”

16. Click OK to proceed.

The Net Property Difference window appears listing a difference in the ROUTE_RRIORITY property on the CLK net in the schematic.

Figure 4-2 Pin Swapping Window

Changing the Property Flow Setup

Overview

In Version 14.0, the Property Flow Setup defines the properties that should be transferred between Concept HDL and Allegro. In the last procedure, you had learned to view the Net Property window, which showed difference in the ROUTE_RRIORITY property on the CLK net in the schematic. The design example in the ds_demos/net_properties/hdli directory had the ROUTE_RRIORITY property defined as transferable between Concept HDL and Allegro.

Important

It is extremely important that you should define all properties that you want to be transferred between Concept HDL and Allegro before you run Design Differences.
Task Overview

You will learn to change the Property Flow Setup by defining the ROUTE_PRIORITY property first as non-transferable and next as transferable.

Steps

   
   The Property Flow Setup dialog box appears.

Figure 4-3 Property Flow Setup Dialog Box
The Property Flow Setup dialog box lists properties and defines whether these properties apply to Concept HDL or Allegro or both. If you want any of these properties to be transferred from Concept HDL to Allegro and back, you need to select its *Transfer* check box.

Notice that the `ROUTE_RRIORITY` property has its *Transfer* check box selected.

2. Clear the *Transfer* check box corresponding to the `ROUTE_RRIORITY` property, and click *OK* to close the dialog box.

A message box appears stating that you have made changes to the property list. You are asked to either reload the Allegro board or update differences.

**Figure 4-4 Design Differences Message Box**


A message box appears displaying the message that the schematic and `route_priority.brd` board file are in sync.

**Exercise**

1. Re-define the `ROUTE_RRIORITY` property as transferable and generate design differences.

2. Load the `max_via_count.brd` board in Design Differences and check the property differences between the schematic and the `max_via_count.brd` board.

3. Define the `MAX_VIA_COUNT` property as non-transferable in the Property Flow Setup dialog box for the `max_via_count.brd` board and then use Design Differences to again check property differences between the schematic and the `max_via_count.brd` board.
Updating the Schematic with the Property Changes in the Board

Task Overview

You will now update the schematic with property differences in the `route_priority.brd` board file. Ensure that the schematic and board are in sync after the update.

Steps

1. Select `File > Load Allegro Board` in Design Differences, and select the `route_priority.brd` board file in the Select Board File to Compare dialog box.
   
   A message box appears with the message “Reload Allegro Board has successfully completed!”

2. Click `OK` to proceed.

   
   The Preview ECO on Schematic dialog box is displayed. The `Property Changes List` displays differences in the `ROUTE_RRIORITY` property.

4. Click `OK` to update the schematic.
   
   The Message log in the Design Differences window is updated and the Import Physical dialog box is displayed.

5. Click `OK`.
   
   A Progress Window appears mentioning that design is netlisted and being fed back. Finally a message box appears asking whether you want to see Packager results.

6. Click `No`.
   
   The Control is passed back to Design Differences, which displays a message that schematic has successfully loaded.

7. Click `OK`.
   
   Packager-XL runs in the feedback mode and updates the packager files. Changes are also made to the Concept HDL schematic. A message box appears displaying the message that the schematic and the `section_swapped_u3-u10.brd` board file are in sync.
8. Click OK to close the message box.

9. Select Tools > Back Annotate in the Concept HDL window to update the Concept HDL schematic with the changes in the packager files using the pstback.dat file.

   Notice that the Package Backannotation check box is selected and the pstback.dat file in the packaged view is selected for backannotation. You also have an option to backannotate electrical constraints. Since the current design does not have any electrical constraints, we will not update them.

10. Click OK.

   Concept HDL schematic is updated with the latest property information from the board.

11. Open the Concept HDL schematic to confirm visually that the schematic has been updated.

12. Select File > Exit in Design Differences, Allegro, Concept HDL, and Project Manager. Do not save any changes.
Synchronizing Component Properties Differences

Objective

To see how differences in component properties are displayed in Design Differences and how they are updated in the schematic.

At the end of this chapter, you will be able to:

- Use Design Differences to view differences caused by changes in component properties.
- Query the logical design or the physical design from Design Differences.
- Update instance property changes to the schematic.

Viewing Component Property Differences

Task Overview

You will open the atm.cpm file in the ds_demos/component_properties/hdli directory in Project Manager, and view the schematic in Concept HDL and the board in Allegro. Compare the differences between the schematic and the u6_props_mod.brd file.

Steps

1. Load the atm.cpm file located in the ds_demos/component_properties/hdli directory in Project Manager.

2. Click on the Design Entry icon in Project Manager to open the schematic in Concept HDL.

   Concept HDL opens the atm.cpm project and displays the schematic.
3. Click on the Layout button in Project Manager to launch Allegro.

4. Select File > Open in Allegro and load the u6_props_mod.brd file.

5. Select Display > Property in Allegro.

   The Show Property dialog box appears.

6. Select the property ROOM, and set the value as CPU.

7. Click on the Show Val button.

   Drag to the bottom of the window to see that the U6 component has the ROOM property with the value CPU.

   Verify that no component in Concept HDL schematic has the ROOM property with the value CPU. You may use the Global Find dialog box and search for the ROOM property with the value CPU. You will find that U6 has the ROOM property with the value CPU. However, the winning value is CNTR.

8. Select Tools > Design Differences in Concept HDL, and if you are asked to expand the design, click Yes.

   The Design Differences dialog box is displayed.

9. Select u6_props_mod as the board, ensure that the Update package view before compare check box is selected, and click OK to start Design Differences.

   The Export Physical dialog box appears. Notice that the Update Allegro Board check box is grayed. You cannot update the board.

10. Click OK to package the design.

   The Progress window appears stating that the design is being netlisted and packaged. After packaging is over message box appears asking whether you want to see Packager results.

Figure 5-1 Design Sync Message Box
11. Click No.

The Control is passed back to Design Differences, which compares the board and the schematic information.

The Instance Property Difference window appears listing differences in the ROOM property. Notice that the ROOM property has the value CNTR in the schematic and the value CPU in the board.

**Figure 5-2 Instance Property Window**

You have verified that differences exists between the sch_1 schematic and the u6_props_mod.brd board file. You will now use Design Differences to find these differences.

**Exploring the Logical and Physical Designs in Design Differences**

**Task Overview**

Design Differences allow you to browse the logical design, that is the schematic, and the physical design, that is the board. You can use Design Differences to browse to any component, net, or part and find any property attached to them.

You will now browse through the physical design and verify the value of the ROOM property attached to the U6 component.

**Steps**

1. Select Explore > Physical Design in Design Differences.

   A window named Board View appears. The board name atm(u6_props_mod.brd) is displayed on the Title Bar.
You will now browse through this window to find out how many components have the `ROOM` property attached and why this property is causing differences.

2. Expand the `Components` branch by clicking at the + button to the left of the `(Components=29)` row.

3. Navigate to the branch `refdes=U6` and expand the `[properties=3]` row.

Notice that the `ROOM` property is attached to the `U6` component. See the Board View Window: Expanded figure below.

Figure 5-4  Board View Window: Expanded
4. Explore another branch. For example, determine how many 74F04 inverters are being used in the design. Expand the branch \(\text{[parts}=14\text{]}\).

5. Select the 74F04 part and expand it by double-clicking it.

Notice that the 74F04 part is a two-pin component with 14 default properties and that there are three such components on the board.

6. Expand the \(\text{[components}=3\text{]}\) row.

The reference designators of the three components appear. You may further expand the rows corresponding to these components and find information about instances and properties of each component.

7. Expand the U16 component.

The U16 component has four instances and three properties attached to it.

8. Expand the \(\text{[instances}=4\text{]}\) row.

9. Expand the first instance with \(\text{path }= 130p\).

Information about pins, instance properties, and the canonical name appears. You may now find information about any of these.

**Note:** If you ever want to find the component that corresponds to a row in Design Differences, you may select the row in Design Differences and select *Highlight Source* in the RMB menu.

10. Select the row corresponding to the canonical name \(\text{cname}@fx.atm\).
11. Display the RMB menu by right-clicking and select *Highlight Source*.

The *Concept HDL: Source Selected* figure on page 53 displays the component corresponding to the canonical name `cname=@fx.atm` highlighted in Concept HDL.

Figure 5-6 Concept HDL: Source Selected
Exercise

Browse the logical design to verify the value of different properties for the U6 component.

Tip

Select Explore - Logical Design and expand the design.

Querying a Design from Design Differences

Task Overview

Query the design for specific properties in both the logical and physical designs. Query the design for an instance that has the ROOM property with the value CNTR attached to it.

Steps

1. Select Explore > Query Design in Design Differences.
   
The Query Design dialog box appears.

Figure 5-7 Query Design Dialog Box

The Query Name field displays existing queries. You can create new queries by clicking on the New button or edit an existing query by clicking on the Edit button.

2. Click New to create a new query.
The Add Query dialog box appears.

Figure 5-8 Add Query Dialog Box

3. Set the following values in the Add Query dialog box:

Query Name = ROOM_CNTR
Design View = Schematic
Find What = Instance
Property Name = ROOM
Value = CNTR

4. Click OK to save the query.

The Query Design dialog box is displayed.

5. Select Find to run the query.

The Query Schematic window appears with all matching instances listed.

**Figure 5-9 Query Schematic Window**

![Query Schematic Window](image)

The first line in the Query Schematic shows the name of the query. Notice that 42 matches are returned.

**Note:** You may expand on any of the instances to see the pin and property details about the instances.

**Exercise**

Query the physical design to locate all instances where the ROOM property has the value CPU.
Hint

Define a new query and select design view as board.

Note: You can have more than one query window open. You can use these windows to compare designs by using specific sets of properties.

Updating the Schematic with Component Property Differences

Task Overview

You will now update the schematic with property differences in the u6_props_mod.brd board file. Ensure that the schematic and board are in sync after the update.

Steps

1. Select File > Load Allegro Board in Design Differences, and select the u6_props_mod.brd board file in the Select Board File to Compare dialog box.

   A message box appears with the message “Reload Allegro Board has successfully completed!”

2. Click OK to proceed.


   The Preview ECO on Schematic dialog box is displayed. The Property Changes List displays differences in the ROOM property.

4. Click OK to update the schematic.

   The Message log in the Design Differences window is updated and the Import Physical dialog box is displayed.

5. Click OK.

   A Progress Window appears mentioning that design is netlisted and being fed back. Finally a message box appears asking whether you want to see Packager results.

6. Click No.

   The control is passed back to Design Differences, which displays a message that schematic has successfully loaded.
7. Click OK.

    Packager-XL runs in the feedback mode and updates the packager files. Changes are also made to the Concept HDL schematic. A message box appears displaying the message that the schematic and the u6_props_mod.brd board file are in sync.

8. Click OK to close the message box.

9. Select Tools > Back Annotate in the Concept HDL window to update the Concept HDL schematic with the changes in the packager files using the pstback.dat file.

    Notice that the Package Backannotation check box is selected and the pstback.dat file in the packaged view is selected for backannotation. You also have an option to backannotate electrical constraints. Since the current design does not have any electrical constraints, we will not update them.

10. Click OK.

    Concept HDL schematic is updated with the latest property information from the board.

11. Confirm visually that the schematic has been updated.

12. Select File > Exit in Design Differences, Allegro, Concept, and Project Manager. Do not save any changes.
Synchronizing Pin Properties Differences

Objective

To see how differences in pin properties are displayed in Design Differences and how they are updated in the schematic.

At the end of this chapter, you will be able to:

- Use Design Differences to view differences caused by changes in pin properties.
- View differences in pin properties between the schematic and the board.
- Save difference information and view the differences later.

Viewing Pin Property Differences

Task Overview

You will open the *atm.cpm* file in the *ds_demos/pin_properties/hdli* directory in Project Manager, and view the schematic in Concept HDL and the board in Allegro. First, compare the differences between the schematic and the *sync.brd* file. Next, compare the differences between the schematic and the *ul6_pin_properties.brd* file.

Steps

1. Load the *atm.cpm* file located in the *ds_demos/pin_properties/hdli* directory in Project Manager.
2. Click on the *Design Entry* icon in Project Manager to open the schematic in Concept HDL.
   
   Concept HDL opens the *atm.cpm* project and displays the schematic.
3. Select *Tools > Design Differences* in Concept HDL, and click *Yes* in the message box.
The Design Differences dialog box is displayed.

4. Select sync.brd as the board, ensure that the *Update package view before compare* check box is not selected, and click OK to start Design Differences.

A message box stating that no differences exist between the schematic and the board (sync.brd) appears. You will now compare whether differences exist between the schematic and the ul6_pin_properties.brd file.

5. Click on the *Layout* button in Project Manager to launch Allegro.

6. Select *File > Open* in Allegro and load the ul6_pin_properties.brd file.

7. Select *Display > Property* in Allegro.

   The Show Property dialog box appears.

8. Select the property *PINUSE*, set the value as *BI*, and click on the *Show Val* button.

   A window appears showing that the U16 and U22 components have the *PINUSE* property with the value *BI*.

9. Verify that the U16 component in Concept HDL schematic does not have the *PINUSE* property with the value *BI*.

10. Select *Difference > Property Flow Setup* in Design Differences.

    The Property Flow Setup dialog box appears.

11. Ensure that the *Transfer* check box corresponding to the *PINUSE* properties selected.

12. Select *File > Load Allegro Board* in Design Differences, and select the ul6_pin_properties.brd board file in the Select Board File to Compare dialog box.

    A message box appears with the message “Reload Allegro Board has successfully completed!”

13. Click OK to proceed.

    The Pin Property Difference window appears.

*Figure 6-1 Pin Property Difference Window*
The Pin Property Difference window lists differences in the PINUSE property. Notice that the PINUSE property has the value BI in the board. This property is not listed in the schematic.

Saving the Output Difference Information

Task Overview

You can save difference information in a text file so that it can be used for future reference. You will also see how you can save the pin property difference that was outputted in the last procedure in a text file. You will also view this file from within Design Differences.

Tip

You can view any text file from within Design Differences.

Steps

1. Ensure that the Pin Property Difference window is active. For this, select Difference > Pin Property in Design Differences.

2. Select File > Output Difference to dump the pin property differences in the pinprop.dif file.

   A text window displays the pinprop.dif file. Notice that this file is generated in the packaged view.

3. Close the pinprop.dif file by clicking on the Close button of the text editor.

   You may open this file and view it from within Design Differences.


   The Choose File browser appears.

5. Select the pinprop.dif file in the packaged view, and click Open.

   The Pin Property Difference File (pinprop.dif) figure on page 63 appears.
Figure 6-2  Pin Property Difference File (pinprop.dif)

Project File: D:\ds_demos\pin_properties\hcl\atm.cpm
Comparison Type: atm(sch_1) vs. atm(u16_pin_properties.brd)
Source Design: atm(sch_1)
Target Design: atm(u16_pin_properties.brd)
Difference Type: pinprop
Number of Differences: 2
Created at: 16:09:00 Sunday, December 03, 2000

<table>
<thead>
<tr>
<th>Name</th>
<th>Schematic Value</th>
<th>Board Value</th>
<th>Pin</th>
<th>Pin #</th>
<th>Section #</th>
<th>RefDes</th>
<th>Part</th>
</tr>
</thead>
<tbody>
<tr>
<td>PINUSE</td>
<td>51</td>
<td>Y&lt;0&gt;</td>
<td>U16.6</td>
<td>3</td>
<td>U16</td>
<td>74F04-</td>
<td></td>
</tr>
<tr>
<td>BASE (fx.atm</td>
<td>sch_1</td>
<td>:page1_131p</td>
<td>y*(0 D)</td>
<td>51</td>
<td>Y&lt;0&gt;</td>
<td>U16.6</td>
<td>3</td>
</tr>
<tr>
<td>BASE (fx.atm</td>
<td>sch_1</td>
<td>:page1_131p</td>
<td>a(C))</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

For Help, press F1

Updating the Schematic with Pin Property Differences

Task Overview

You will now update the schematic with the pin property differences in the u16_pin_properties.brd board file. Ensure that the schematic and board are in sync after the update.

Steps

1. Select File > Load Allegro Board in Design Differences, select the u16_pin_properties.brd board file in the Select Board File to Compare dialog box, and click OK to proceed.

2. Select Sync > Update Concept Schematic in Design Differences.

   The Preview ECO on Schematic dialog box is displayed. The Property Changes List displays differences in the ROOM property.

3. Click OK to update the schematic.
The Message log in the Design Differences window is updated and the Import Physical dialog box is displayed.

4. Click OK.

A Progress Window appears mentioning that design is netlisted and being fed back. Finally a message box appears asking whether you want to see Packager results.

5. Click No.

The Control is passed back to Design Differences, which displays a message that schematic has successfully loaded.

6. Click OK.

Packager-XL runs in the feedback mode and updates the packager files. Changes are also made to the Concept HDL schematic. A message box appears displaying the message that the schematic and the u16_pin_properties.brd board file are in sync.

7. Click OK to close the message box.

**Taking New Pin Properties to the Board**

**Task Overview**

You can take a new pin property into the board. You will now define a new property, LEAD_RESISTANCE, in the schematic, and then take it to the board.

**Steps**

1. Select Text > Attributes in Concept HDL.

2. Select the U16.5 pin and attach the LEAD_RESISTANCE property with the value 0.005 to it.

   You will now take this property to the board.

3. Select File > Save in Concept HDL to save the schematic.

4. Select File > Export Physical to package the design.

   The Export Physical dialog box appears.
5. Select only the Package Design option, set the option to Preserve, and click OK to package the design.

   A message box appears stating that packaging has finished successfully and asks if you want to check the results.

6. Select Yes.

7. Click on the View Results button and select the pstxnet.dat file.

   The pstxnet.dat file opens in a text editor.

8. Search for the text LEAD_RESISTANCE in the file.

   The LEAD_RESISTANCE property is defined in the file.
9. Exit the text editor, and close the progress window.
   You need to define the \texttt{LEAD\_RESISTANCE} property on the board.

10. Open the \texttt{u16\_pin\_properties.brd} board in Allegro.

11. Select \textit{Setup} > \textit{Property Definitions}.
   The Define User Properties dialog box appears.

\textbf{Figure 6-4 Define User Properties Dialog Box}

12. Type \texttt{LEAD\_RESISTANCE} as the property name in the \textit{Name} field, and click \textit{OK}.

13. Select \textit{Pins} as the \textit{Data Elements}, \texttt{STRING} as the \textit{Data Type}, and click \textit{OK}.

14. Select \textit{File} > \textit{Save As} and save the board as \texttt{lead\_resistance.brd}.

15. Select \textit{Display} > \textit{Property} in Allegro.

16. Select the \texttt{LEAD\_RESISTANCE} property and click \textit{Show Val}.
   The following message appears in the Allegro console window:
   \texttt{W- No Instances of property LEAD\_RESISTANCE found.}
You will now import the schematic into this board.

17. Select File > Import - Logic.

    The Import Logic dialog box appears.

**Figure 6-5 Import Logic Dialog Box**

18. Select HDL-Concept radio button, the packaged directory in the Import directory field, and click on the Import Cadence button.


20. Select the property LEAD_RESISTANCE, and click on the Show Val button.

    A window appears showing that U16.5 pin has the LEAD_RESISTANCE property with the value 0.005.
Synchronizing Differences Caused By New Properties in Allegro

Task Overview

You will now edit the LEAD_RESISTANCE property in the lead_resistance.brd board, and then synchronize the schematic using Design Differences.

Steps

1. Select Edit > Properties in Allegro and ensure that only the Pins check box is selected in the Find Filter.
2. Click More and select Property in Object Type.
3. Select LEAD_RESISTANCE = 0.005 and click OK.

   The Edit Property dialog box appears. You can edit the property in this dialog box.
4. Select the LEAD_RESISTANCE property, type the value 0.010, and click Apply.

   Notice that the property value has changed in the Show Properties window.
5. Click OK to close the Edit Property window.
6. Save the board with the name lead_resistance_changed.brd.
7. Select Difference > Property Flow Setup in Design Differences.

   The Property Flow Setup dialog box appears.

   If the LEAD_RESISTANCE property is not available in the properties list, then click Add and define a new property named LEAD_RESISTANCE and define it as transferable between the schematic and the board.
8. Click OK to close the Property Flow Setup dialog box, and click OK to close the message box
9. Close Design Differences and open it again.
10. Select the lead_resistance_changed.brd board file in the Allegro Board field, ensure that the Update package view before compare check box is selected, and click OK to proceed.

   The Export Physical dialog box appears with the Package Design check box selected.
11. Click OK.

A Progress Window appears mentioning that design is netlisted and being fed back. Finally a message box appears asking whether you want to see Packager results.

12. Click No.

The Control is passed back to Design Differences, which displays a message that schematic has successfully loaded.

Design Differences shows that the value of the LEAD_RESISTANCE property on the board is 0.010, while the value on the schematic is 0.005.


The Preview ECO on Schematic dialog box appears.
14. Click OK to update the schematic.
   The Message log in the Design Differences window is updated and the Import Physical dialog box is displayed.

15. Click OK.
   A Progress Window appears mentioning that design is netlisted and being fed back. Finally a message box appears asking whether you want to see Packager results.

16. Click No.
   The control is passed back to Design Differences, which displays a message that schematic has successfully loaded.
17. Click OK.

Packager-XL runs in the feedback mode and updates the packager files. Changes are also made to the Concept HDL schematic. A message box appears displaying the message that the schematic and the lead_resistance_changed.brd board file are in sync.

18. Click OK to close the message box.

19. Open the Concept HDL schematic to confirm visually that the schematic has been updated.

20. Select File > Exit in Design Differences, Allegro, Concept HDL, and Project Manager. Do not save any changes.
Handling Bypass Capacitors

Objective

To see how netlist differences caused by the addition of new components, such as bypass capacitors, on the board are displayed in Design Differences and how they are updated in the schematic.

At the end of this chapter, you will be able to:

1. Use Design Differences to view differences caused by the addition of bypass capacitors.
2. Use Design Association to migrate the connectivity changes to the schematic.

Viewing Connectivity Differences

Task Overview

You will open the atm.cpm file in the ds_demos/bypass_cap/hdli directory in Project Manager, and view the schematic in Concept HDL and the board in Allegro. First, compare the differences between the schematic and the sync.brd file. Next, compare the differences between the schematic and the bypass_cap.brd file.

Steps

1. Load the atm.cpm file located in the ds_demos/bypass_cap/hdli directory in Project Manager and launch Concept HDL from Project Manager.
2. Select Tools > Design Differences in Concept HDL, and click Yes in the message box. The Design Differences dialog box is displayed.
3. Select sync.brd as the board, and click OK to start Design Differences.
A message box stating that no differences exist between the schematic and the board (sync.brd) appears.

4. Click OK to close the message box.

You will now compare whether differences exist between the schematic and the bypass_cap.brd file.

5. Click on the Layout button in Project Manager to launch Allegro.

6. Select File > Open in Allegro and load the sync.brd board file.

Note that there is only one capacitor, called CAP1, placed on the lower middle part of the board.

7. Select File > Open in Allegro and load the bypass_cap.brd board file.

If you search for capacitors in this board, you will find that there are four capacitors, named CAP1, CAP2, CAP3, and CAP4, placed on the lower middle part of the board. The capacitors are connected between VCC and GND.

8. Select File > Load Allegro Board in Design Differences, and select the bypass_cap.brd board file in the Select Board File to Compare dialog box.

A message box appears with the message “Reload Allegro Board has successfully completed!”

9. Click OK to proceed.

The Instance Difference Window on page 73 and Pin-net Connection Difference Window on page 74 appear.

Figure 7-1 Instance Difference Window

<table>
<thead>
<tr>
<th>Instance</th>
<th>Part Name</th>
<th>Schematic RefDes</th>
<th>Board RefDes</th>
<th>Section #</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>CAPACITOR</td>
<td>CAPACITOR</td>
<td>CAP2</td>
<td>1</td>
<td></td>
<td>@</td>
</tr>
<tr>
<td>CAPACITOR</td>
<td>CAPACITOR</td>
<td>CAP3</td>
<td>1</td>
<td></td>
<td>@</td>
</tr>
<tr>
<td>CAPACITOR</td>
<td>CAPACITOR</td>
<td>CAP4</td>
<td>1</td>
<td></td>
<td>@</td>
</tr>
</tbody>
</table>

The Instance Difference window lists CAP2, CAP3, and CAP4 as extra instances in the board. The components available on the board are shown in red. The field below the Schematic RefDes is empty, which indicates that these components are not available on the schematic.
Figure 7-2 Pin-net Connection Difference Window

The Pin-net Connection Difference window lists the differences in the pin-net connections in the schematic and the board. Differences exist for pin names A<0> and B<0>. The Pin-Net connection Difference window shows the nets that are connected differently from the schematic. There are six rows for the six new pin-net connections.

Writing the Marker File

Task Overview

You will write the connectivity changes in a file called dessync.mkr. Design Association uses this file to update the Concept HDL schematic.

Steps

1. Select Sync > Update Concept Schematic to launch the Preview ECO on Schematic dialog box.

   The Preview ECO on Schematic Dialog Box on page 75 appears.
Figure 7-3  Preview ECO on Schematic Dialog Box

Notice that the top section of the dialog box shows the changes that need to be carried out in the schematic. This section shows that three actions requiring addition of an instance to the schematic need to be carried out.

2. Clear the **Click OK button to launch Design Association to feedback connectivity changes to Schematic check box**. Click **OK**.

Design Association appears with the marker file loaded. See **Design Association** on page 76. Notice that three actions that need to be executed are shown in three lines.
3. Select **Explore > Logical Design** to display the schematic view.

   The Schematic View window appears. Notice that the total number of components is 30.

4. Select **Explore > Physical Design** to display the schematic view.

   The Board View window appears. Notice that the total number of components is 33. You can explore both the logical design and physical designs from Design Differences.

5. Select **File > Exit to close Design Differences**.
Updating the Concept HDL Schematic Using Design Association

Task Overview

You will use Design Association uses file to update the Concept HDL schematic with connectivity.

Steps

1. Select the first marker.
   
   Notice that the number of the action selected is shown on the window in the format “Markers: 1(3).”

2. Click on the Execute button.
   
   A window pops up displaying the message that place component in Concept.

Figure 7-5 Design Association Message Window

3. Click OK.
   
   A component is attached to the cursor as in an add component operation.

4. Select an empty location on the schematic, and click the left mouse button to place the component.
   
   The following window pops up displaying the message that version 0 is illegal and that Concept HDL is using version 1.
5. Click **OK**.
   As soon as you place the component, you will see that signal names are automatically attached to the pins.

6. Zoom into the location to view the signal names.
   You will also notice that a blue cross is placed in the Design Association window against the action to indicate that the action has completed successfully.

7. Select **Text > Attributes**, and select the capacitor. Set the value to 50nf.
   Note that the location property is set to **CAP2**.

8. Click **OK** to dismiss the attribute window.

9. Type a semicolon (;) in the Concept HDL console window and press Enter to finish the attribute command.

10. Repeat steps 2-9 to place the other two capacitors in on the Concept HDL schematic. Set the value of both capacitors to **50nf**.

   **Note**: It is important to assign a value to capacitors because you cannot save the schematic until all markers are assigned values.

11. Select **File > Save** to save the schematic.

12. Select **File > Export Physical** to package the design.
   The Export Physical dialog box appears.

13. Select the **Package Design** check box. Set the option to **Preserve**.

14. Select the **Update Allegro Board** check box.

15. Click **OK** to package the design.
A progress window appears. When the design is packaged, a pop-up window appears stating that packaging has finished successfully and asks if you want to check the results.

16. Select No.

17. Select Design Sync > Design Differences in Project Manager.

   The Design Differences dialog box appears. Ensure that only the Update board view before compare check box is selected.

18. Click OK.

   A window appears stating that no differences are detected between the schematic and the board.

   Now the schematic and the board are in sync.

19. Select File > Exit in Design Differences, Allegro, Concept HDL, and Project Manager. Do not save any changes.
Handling Series Terminators

Objective

To see how netlist differences caused by the addition of series terminators on the board are seen in Design Differences and how they are updated to the schematic.

At the end of this chapter, you will be able to:

- Use Design Differences to view differences caused by the addition of series terminators.
- Use Design Association to update the addition of series terminators in the board back to the schematic.

Viewing Connectivity Differences Caused by Series Terminator Additions

Task Overview

You will open the atm.cpm file in the ds_demos/series_term/hdli directory in Project Manager, and view the schematic in Concept HDL and the board in Allegro. First, compare the differences between the schematic and the sync.brd file. Next, compare the differences between the schematic and the ser_term.brd file.

Steps

1. Load the atm.cpm file located in the ds_demos/series_term/hdli directory in Project Manager and launch Concept HDL from Project Manager.
2. Select Tools > Design Differences in Concept HDL, and click Yes in the message box.
   The Design Differences dialog box is displayed.
3. Ensure that only the *Update board view before compare* check box is selected. Select `sync.brd` as the board, and click *OK* to start Design Differences.

A message box stating that no differences exist between the schematic and the board (`sync.brd`) appears. You will now compare whether differences exist between the schematic and the `ser_term.brd` file.

4. Click on the *Layout* button in Project Manager to launch Allegro.

5. Select *File > Open* in Allegro and load the `sync.brd` board file.

Note that there is only one capacitor, called `CAP1`, placed on the lower middle part of the board.

6. Select *File > Open* in Allegro and load the `ser_term.brd` board file.

Note that there is a component called `TERM2` placed on the lower middle part of the board. This component is a series terminator on the net `INTER_SIG`. One end of the resistor is attached to the pin `U16.6` and the other end is attached to the pin `U16.9`.

The following figure shows the change that occurred on the board, then you will see how this change is displayed in Design Differences.

**Figure 8-1 Board State: Before and After Addition of Series Terminator**

![Diagram of board state before and after addition of series terminator.](image)

7. Select *File > Load Allegro Board* in Design Differences, and select the `ser_term.brd` board file in the Select Board File to Compare dialog box.

A message box appears with the message “Reload Allegro Board has successfully completed!”
8. Click OK to proceed.

Four windows appear in Design Differences. These windows are: the Message Log window, the Instance Difference window, the Net Difference window, and the Pin-Net Connection Difference window.

The Pin-net Connection Difference window shows the difference caused by the addition of the series terminators.

Figure 8-2  Pin-net Connection Difference Window

![Pin-net Connection Difference Window](image)

The Instance Difference Window shows that the board has one component that is not present on the schematic.

Figure 8-3  Instance Difference Window

![Instance Difference Window](image)

The Net Difference Window shows that the board has one component that is not present on the schematic.

Figure 8-4  Net Difference Window

![Net Difference Window](image)
Synchronizing Series Terminator Additions in the Schematic

Task Overview

You will use Design Association to synchronize the schematic with the changes caused by the addition of series terminators in the board.

Steps

1. Select Sync > Update Concept Schematic to display the Preview ECO window.
   
   The Preview ECO on Schematic Dialog Box figure on page 84 appears. The Top section of the Preview ECO window shows the changes that need to be carried out in the schematic. Notice that the action involves adding an instance to the schematic.
2. Select the **Click OK button to launch Design Association to feedback connectivity changes to Schematic** check box and click **OK**.

   The Design Association figure on page 85 appears. Notice that the correct marker file is loaded.
3. Select the *Add Series Terminator* action by clicking on it.

   The target pin is highlighted.

4. Click *Execute* to perform the action.

   A message box appears requesting you to select the wire in Concept HDL.

5. Click *OK*.

   As soon as you click on execute a resistor is attached to your cursor. You need to now carefully place this resistor on the schematic in a similar manner as it is placed on the board.
6. Place the resistor on the wire with the \texttt{INTER\_SIG} signal as shown in Figure 8-7 on page 86.

**Figure 8-7 Concept HDL Design Before Execution of Action**

![Image of Concept HDL Design Before Execution of Action]

The resistor is embedded into the wire like in the board.

\textbf{Caution}

*Please ensure that you place the resistor as shown in the following figure failing which you may continue to have design differences between the schematic and the board.*

**Figure 8-8 Concept HDL Design After Execution of Action**

![Image of Concept HDL Design After Execution of Action]

\textbf{After execution of action}

7. Select \textit{File > Save} to save the schematic.

8. Select \textit{File > Export Physical} to package the design.

The Export Physical dialog box appears.
9. Select only the *Package Design* option.

10. Set the packaging option to *Preserve*, and click *OK* to package the design.

    A progress window appears stating that packaging has finished successfully and asks if
    you want to check the results.

11. Select *No* to close the window.

12. Select *File > Exit* in Design Differences, Design Association, Allegro, Concept HDL, and
    Project Manager. Do not save any changes.
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