Contents

1 Introduction
   The Challenge: Power Integrity in High Speed ................................. 5
   PCB Design ............................................................................... 6
   The Solution: SPECCTRAQuest Power Integrity ........................................ 7
   SPECCTRAQuest Power Integrity Workflow ............................................... 7
   Use Models ............................................................................. 11

2 Preparing for Powerplane Analysis ...................................................... 13
   Using the Setup Wizard ................................................................... 14
   Invoking the Setup Wizard .............................................................. 15
   Board Outline ........................................................................... 16
   Stack-up .................................................................................. 17
   DC Net/Plane Association .............................................................. 19
   DC Power Pair Setup .................................................................... 21
   Library Setup ........................................................................... 22
      Choosing a Decoupling Capacitor Library ......................................... 23
      Choosing a Decoupling Capacitor ..................................................... 23
      Modifying a Decoupling Capacitor .................................................. 26

3 Power Integrity Design and Analysis .................................................. 31
   Powerplane Target Impedance ......................................................... 32
   Single-Node Simulation ................................................................ 33
      Overview ................................................................................ 33
      Running a single-node simulation ................................................ 34
      Working in the worksheet ............................................................... 36
# SPECCTRAQuest Power Integrity Design Guide

## Contents

**Analysis** ................................................................. 38  
  - Analysis Waveforms .................................................. 38  
**Reports** ............................................................... 40  
**Multi-Node Simulation** .................................................. 42  
  - Gridding Planes for Multi-node Simulation ......................... 42  
**Analysis Preferences** .................................................. 43  
**Placing Components** ................................................... 46  
**Placing the Voltage Regulator Module (VRM)** ......................... 47  
**Placing Noise Sources** ................................................ 48  
**Placing Decoupling Capacitors** ....................................... 50  
  - Pre-Placement Operations ........................................... 51  
  - Post-Placement Operations ......................................... 53  
  - Crossprobing ......................................................... 54  

### A

**Temporary Packages** .................................................. 55  
**Overview** ............................................................ 56  
**Creating Temporary Surface Mounted Packages** ....................... 56  
**Creating Temporary Leaded Packages** ................................ 59  

### B

**Voltage Regulator Module (VRM)** .................................... 61  
**Working with the Voltage Regulator Module** .......................... 62  
**Voltage Regulator Module Editor** .................................... 63  
................................................................. 65
Introduction

Topics in this chapter include

- The Solution: SPECCTRAQuest Power Integrity on page 7.
- SPECCTRAQuest Power Integrity Workflow on page 7.
- Use Models on page 11.
The Challenge: Power Integrity in High Speed PCB Design

As clock and data frequencies increase and high-speed systems become more densely populated, noise-free power delivery becomes a major challenge for PCB design. When fast switching devices change state simultaneously, power flow ripple propagates through the power delivery system as noise that varies with frequency. This noise can, in turn, disturb surrounding high-speed devices.

Important

Without adequate power, high-speed components behave unpredictably.

To ensure that high-speed systems continue to deliver the required performance at these new levels, power delivery impedance has to be controlled over a wider range of frequencies. This is accomplished through careful consideration of the design of the switching power supply, bulk capacitance, ceramic capacitance, and power and ground plane-pairs over the frequencies of interest.

Figure 1-1 shows where, in the frequency spectrum, each component in the power delivery system is most effective at controlling target impedance.

Important

Capacitors provide (1), a local source of voltage for nearby active devices and (2), a low impedance path to ground for noise.

![Figure 1-1 Components in a Power Delivery System](image-url)
Decoupling capacitors provide a local source of charge for drivers requiring a significant amount of supply current in response to logic switching.

Tip

Capacitors exhibit parasitic inductance that limits their effective frequency range; therefore, you should explore mounting methods that help to minimize inductance.

The Solution: SPECCTRAQuest Power Integrity

SPECCTRAQuest Power Integrity aids you in designing, modeling, and analyzing the PCBs power delivery system. SPECCTRAQuest Power Integrity models plane structures (including connecting vias), synthesizes the number of decoupling capacitors, and analyzes for the physical effects of in-circuit decoupling capacitor placement.

SPECCTRAQuest Power Integrity Workflow

The high-level workflow consists of the following phases:

1. Set up the board database for analysis.
2. Define the target impedance.
3. Perform single-node analysis to validate and refine your capacitor selection.
4. Perform multi-node analysis to refine your placement.

Table 1-1 provides a task breakdown for each phase.
### Table 1-1 Workflow Tasks

<table>
<thead>
<tr>
<th>Task</th>
<th>Phase</th>
<th>For more information see</th>
</tr>
</thead>
<tbody>
<tr>
<td>You use the setup wizard to step through the tasks required to set up the board database for power integrity analysis. Tasks in this phase include:</td>
<td>Phase 1 Database Setup</td>
<td>“Preparing for Powerplane Analysis” on page 13. “Temporary Packages” on page 55.</td>
</tr>
<tr>
<td>■ Creating or importing a board outline</td>
<td></td>
<td></td>
</tr>
<tr>
<td>■ Specify a layer cross-section</td>
<td></td>
<td></td>
</tr>
<tr>
<td>■ Associating plane shapes with DC voltages</td>
<td></td>
<td></td>
</tr>
<tr>
<td>■ Mating plane pairs</td>
<td></td>
<td></td>
</tr>
<tr>
<td>■ Choosing decoupling capacitors</td>
<td></td>
<td></td>
</tr>
<tr>
<td>You establish a target impedance by specifying simulation parameters such as powerplane voltage rails, ripple tolerance, and the worst-case dynamic current. With this information, SPECCTRAQuest Power Integrity then recommends the number of capacitors needed to maintain a target impedance. Tasks in this phase include:</td>
<td>Phase 2 Define the target impedance</td>
<td>“Powerplane Target Impedance” on page 32.</td>
</tr>
<tr>
<td>■ Selecting a plane-pair to analyze</td>
<td></td>
<td>“Working in the worksheet” on page 36.</td>
</tr>
<tr>
<td>■ Specifying a ripple tolerance</td>
<td></td>
<td></td>
</tr>
<tr>
<td>■ Specifying a maximum delta current</td>
<td></td>
<td></td>
</tr>
<tr>
<td>■ Specifying parameters for the voltage regulator module</td>
<td></td>
<td>“Working with the Voltage Regulator Module” on page 62.</td>
</tr>
</tbody>
</table>
### Table 1-1 Workflow Tasks

<table>
<thead>
<tr>
<th>Task</th>
<th>Phase</th>
<th>For more information see</th>
</tr>
</thead>
</table>
| You run a single-node simulation to validate how well your capacitor selection maintains the target impedance. Single-node simulation entails subcircuit extraction from a single point on the board. Decoupling capacitors are considered but their placement is not. Powerplane analysis is performed under ideal conditions. Tasks in this phase include: | **Phase 3** Single-Node Analysis | “Powerplane Target Impedance” on page 32.  
“Single-Node Simulation” on page 33. |
| ■ Selecting a plane-pair to analyze                                   |                        | “Working in the worksheet” on page 36.                                                    |
| ■ Specifying a ripple tolerance                                       |                        | “Working with the Voltage Regulator Module” on page 62.                                   |
| ■ Specifying a maximum delta current                                  |                        | “Running a single-node simulation” on page 34.                                            |
| ■ Specifying parameters for the voltage regulator module              |                        | “Working in the worksheet” on page 36.                                                    |
| ■ Simulating to validate capacitor selection.                        | Phase 4 Multi-Node Analysis | “Analysis” on page 38.                                                                     |
| You refine capacitor placement in the board layout through subcircuit extraction from a multiple points on the board. SPECCTRAQuest Power Integrity considers decoupling capacitor placement in powerplane analysis. Tasks in this phase include: | | “Multi-Node Simulation” on page 42.  
“Gridding Planes for Multi-node Simulation” on page 42 |
| ■ Setting analysis preferences                                        |                        | “Analysis Preferences” on page 43.                                                        |
## Table 1-1 Workflow Tasks

<table>
<thead>
<tr>
<th>Task</th>
<th>Phase</th>
<th>For more information see</th>
</tr>
</thead>
<tbody>
<tr>
<td>Selecting a plane-pair to analyze</td>
<td><strong>Phase 4</strong></td>
<td>“Powerplane Target Impedance” on page 32.</td>
</tr>
<tr>
<td></td>
<td>Multi-Node Analysis (continued)</td>
<td>“Single-Node Simulation” on page 33</td>
</tr>
<tr>
<td>Specifying a ripple tolerance</td>
<td></td>
<td>“Working with the Voltage Regulator Module” on page 62</td>
</tr>
<tr>
<td>Specifying a maximum delta current</td>
<td></td>
<td>“Analysis” on page 38.</td>
</tr>
<tr>
<td>Specifying parameters for the voltage regulator module</td>
<td></td>
<td>“Placing Components” on page 46.</td>
</tr>
<tr>
<td>Evaluating an impedance profile</td>
<td></td>
<td>“Crossprobing” on page 54</td>
</tr>
<tr>
<td>Placing noise sources</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Placing decoupling capacitors</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Crossprobing</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Use Models

You can employ SPECCTRAQuest Power Integrity in the following phases of floorplanning:

■ Exploration

In the *exploration* phase, the board has no components placed and there may *not* be a netlist available. The board outline, plane shapes, DC net assignments, and layer stack-up may *not* be in place as well. SPECCTRAQuest Power Integrity comes with a setup wizard that guides you through the necessary steps to prepare the board for power integrity analysis.

☑ See Chapter 2, “Preparing for Powerplane Analysis,” for information on using the setup wizard.

■ Design

In the *design* phase, the board has components placed but the board is not routed. If the requisite parameters are in place, you can refine placement and continue with power integrity design and analysis. If one or more the requisite parameters are not in place, the setup wizard appears automatically so you can specify the missing set-up information.

☑ See Chapter 2, “Preparing for Powerplane Analysis,” for information on using the setup wizard.

☑ See Chapter 3, “Power Integrity Design and Analysis,” for information on using the Power Integrity Design and Analysis dialog box.

■ Verification

In the *verification* phase, the board has components placed and the board is routed. In this phase, you refine placement through power integrity analysis.

☑ See Chapter 3, “Power Integrity Design and Analysis,” for information on using the Power Integrity Design and Analysis dialog box.
Preparing for Powerplane Analysis

Topics in this chapter include

- Using the Setup Wizard on page 14.
- Board Outline on page 16.
- Stack-up on page 17.
- DC Net/Plane Association on page 19.
- DC Power Pair Setup on page 21.
- Library Setup on page 22.
Using the Setup Wizard

The board database must contain the following information before SPECCTRAQuest Power Integrity can analyze the board's power delivery system.

You must specify the:

- Board outline
- Layer stackup
- Power plane shapes
- DC nets associated with the power planes
- Power and ground plane pairs
- Capacitor library models

SPECCTRAQuest Power Integrity provides the setup wizard to guide you through the preparation process. You can invoke the setup wizard directly from the Power Integrity Design and Analysis dialog box. See “Power Integrity Design and Analysis” on page 31 for more information about using the Power Integrity Design and Analysis dialog box. SPECCTRAQuest Power Integrity spawns the setup wizard when additional information is required.

⚠️ Important

Parameters that you specify in the Power Integrity Setup Wizard (by choosing Analyze – Power Integrity) are independent from the parameters that you specify in the Board Setup Wizard (by choosing Board – Setup Advisor).
Invoking the Setup Wizard

You start the setup wizard from the floorplanner by choosing Analyze – Power Integrity.

- If the database requires information to perform power integrity analysis, the initial screen of the setup wizard appears as shown in Figure 2-1 on page 15.

- If the database contains the requisite data to perform power integrity analysis, the Power Integrity Design and Analysis dialog box appears from which you can begin power integrity analysis. You can navigate to the setup wizard from the Power Integrity Design and Analyze dialog box if you want to change the setup information. See “Power Integrity Design and Analysis” on page 31 for information on using the Design and Analysis dialog box.

Figure 2-1  Setup Wizard (Initial Screen)

➤ Click Next to proceed to the board outline screen in the setup wizard.
Board Outline

SPECCTRAQuest Power Integrity requires a board outline for placement and plane model extraction. If an outline does not exist, or if it is incomplete, a message displays in the upper-right corner of the screen.

![Figure 2-2 Setup Wizard (Board Outline Screen)](image)

You can create an outline from scratch or you can import one from another design. Once in place, a representation of the outline appears in the upper-right corner of the screen. You can also edit the outline to suit your needs.

**Tip**

When you click *Edit Outline*, the board outline confirmer appears as the current board outline opens in the floorplanner view. In the confirmer, click *Edit* and then click and drag the resize handles to change the size or the shape of the outline. In the confirmer, click *OK* to accept the new outline.

➤ Click *Next* to proceed to the *board Stack-up* screen in the setup wizard.
Stack-up

SPECCTRAQuest Power Integrity requires a layer stack-up to calculate the power pair separation used to generate plane models. If a stack-up does not exist, or if it does not contain plane layers, a message displays in the upper-right corner of the screen.

![Stack-up Screen](image)

**Figure 2-3 Setup Wizard (Stack-up Screen)**

You can modify a stack-up (click the *Edit – Stack-up* button) or you can import one from another design (click the *Import – Stack-up* button).

**Tip**

When importing a stack-up, SPECCTRAQuest Power Integrity looks for board files associated with the `STACKUP_PATH` environment variable.
Once in place, a representation of the stack-up appears in the upper-right corner of the screen (see Figure 2-4).

![Topological View](image1) ![Physical View](image2)

**Figure 2-4 Viewing the Layer Stack-up**

In *topological view*, the stackup (signal, plane, dielectric) appears uniformly. In *physical view*, the stackup appears proportionally.

➤ Click *Next* to proceed to the *DC Net/Plane Association* screen in the setup wizard.
DC Net/Plane Association

SPECCTRAQuest Power Integrity requires a DC voltage assignment on each plane shape before it can wire the decoupling capacitors. In this screen, you can modify an existing voltage assignment or you can specify a new one. You can also edit the plane shape.

Figure 2-5  Setup Wizard (DC Net/Plane Association)

The same layer can have many plane shapes. In power integrity analysis, you may choose to ignore certain plane shapes, such as smaller ones.

SPECCTRAQuest Power Integrity lets you specify minimum plane/board area (area ratio) in the Power Integrity tab of the analysis preferences dialog box (choose Analyze – Analyze Preferences). On conductor layers, any plane less than this area ratio is not listed in the DC Net Plane Association screen of the setup wizard. SPECCTRAQuest Power Integrity always considers plane shapes on plane layers. All other layers must have a DC net association. Split planes on the same layer will contain plane shapes of differing voltage levels. Each shape, therefore, is associated with a different DC net. See Figure 2-7 on page 22 to learn about plane designators.

Although you can associate DC voltages with plane shapes directly in the wizard, SPECCTRAQuest Power Integrity provides alternative methods to achieve the same effect. The buttons located in the lower-right corner of the screen operate as follows:
Click this button . . . To display the . . .

DC nets **Netlist – Identify DC Nets** dialog box from which you specify power pins and voltage levels.

SPECCTRAQuest Power Integrity does not require you to specify individual voltage pins in a net. It only needs to know about the voltage level on the net so that it can associate the voltage with a plane shape.

**Tip**

Because you can change the voltage directly in the wizard, you do not have to use this dialog box unless you are interested in reviewing all the nets that exist in the design as the wizard shows only those nets that have an attached **VOLTAGE** property.

Edit shape **Board – Plane Outline** dialog box.

➤ Click *Edit* then drag the resizing handles to change the dimensions of the active shape.

**Caution**

*Be aware that deleting, replacing, resizing, or moving a plane shape may adversely impact a paired plane. See DC Power Pair Setup on page 21 for information on paired planes.*

Edit nets **Netlist – Edit Nets** dialog box from which you can create a new net or change the pins in an existing net.

**Tip**

Because you can change the net—or create a new net—directly in the wizard, you do not have to use this dialog box unless you are interested in changing the pins in a net.

➤ Click *Next* to proceed to the *DC Power Pair Setup* screen in the setup wizard.
DC Power Pair Setup

Before power integrity analysis is performed, power and ground planes must be paired. The same ground plane can be shared with one or more power rails—as separate plane pairs—however, only one plane pair is analyzed at a time.

**Figure 2-6 Setup Wizard (Power Pair Setup screen)**

*Tip*

Although not a requirement, you should pair-up planes that are close to each other in the layer stackup.
Each plane is uniquely identified by the name of the plane shape, the name of the layer that contains the plane shape, and the name of the net associated with the plane shape (see “DC Net/Plane Association” on page 19).

![Diagram of [S3] VDD (VDD_3V)](image)

**Figure 2-7  Powerplane Designators**

Once you have selected planes to pair, the calculated inter-plane capacitance displays in the planes section of the power pair setup screen.

- Click Next to proceed to the library setup screen in the setup wizard.

**Library Setup**

SPECCTRAQuest Power Integrity requires access to both ceramic and bulk decoupling capacitor models before analyzing for power delivery problems.

A decoupling capacitor is represented as a device. The device file includes the package model that describes the capacitor’s layout and pin escapes, the capacitor’s part number, a signal model that specifies the capacitor’s value as well as its intrinsic- and nominal mounted inductance, and its equivalent series resistance (ESR).

The library browser categorizes capacitor families by operating characteristics such as capacitance value, physical size and durability, mounting type, and temperature and humidity factors. The .dcl file specifies capacitor family grouping.

Library setup, the last phase in the setup wizard, entails the following functions.

- Choosing a decoupling capacitor library
- Choosing a decoupling capacitor
- Modifying a decoupling capacitor (optional)
Choosing a Decoupling Capacitor Library

You select decoupling capacitor families using the Signal Analysis Library Browser (click Library in the setup wizard, see Figure 2-8 on page 24).

Tip

When searching for decoupling capacitor models, SPECCTRAQuest Power Integrity looks to the directories associated with the DCLPATH environment variable.

In selecting a library, you should choose a family of capacitors whose resonant frequencies cover your design’s operating frequency band.

Important

Decoupling capacitor models have specific parameters beyond the capacitors in the default ESPICE device library.

Choosing a Decoupling Capacitor

You select a decoupling capacitor by opening the folder that represents the capacitor family. Once expanded, you can select decoupling capacitors in the family from the capacitor tree. As you click on a capacitor, its resonant frequency appears as a vertical mark on a frequency axis as shown in Figure 2-8 on page 24. The height of this vertical mark represents the capacitor’s ESR. Any capacitor that you select (by clicking its checkbox) is included in downstream analysis and placement.
You want to choose capacitors that cover the frequency band that will yield the desired target impedance for the board.

You can click on a capacitor and then right-click to invoke the context pop-up menu from which you can choose to graph the impedance versus frequency curves of a single capacitor or a group of capacitors. You can also create a new capacitor that represents your specific design requirements.

1. Click on a capacitor.
2. Right-click.
3. Choose a command from the context menu.

Figure 2-8 Context menu choices for decoupling capacitors
Tip

Rather than working with capacitors one-by-one, you can right-click on a folder to quickly enable (check) or disable (uncheck) all capacitors in the library tree.

The frequency versus impedance curves (see Figure 2-9 on page 25) depict the capacitive effects as shown by the upward slope of the curve and the inductive effects as shown by the downward slope of the curve. The knee of the curve depicts the equivalent series resistance, or the capacitor’s resonant frequency.

Important

The capacitor’s resonant frequency is the point of least impedance and, therefore, the point at which the capacitor is most effective at replenishing current to the board. Below the resonant frequency, the capacitor’s impedance is predominantly capacitive; above the resonant frequency, the capacitor’s impedance is predominantly inductive.

Figure 2-9  Frequency versus impedance graph of selected capacitors
Modifying a Decoupling Capacitor

You use the Decoupling Capacitor Editor to view or modify the characteristics of the selected decoupling capacitor.

➤ To access the Decoupling Capacitor Editor, click on a capacitor in the library tree, right-click, and choose Edit from the context pop-up menu.

Any changes that you make in the Decoupling Capacitor Editor are saved to the device model file that is associated with the selected capacitor. All capacitors that reference the device model, in turn, are refreshed with the new values.

Important

If the device model file is write-protected, your edits are saved to the devices.dml file in the current working directory.

![Decoupling Capacitor Editor](image-url)

Figure 2-10 Decoupling Capacitor Editor
**Table 2-1 Using the Decoupling Capacitor Editor**

<table>
<thead>
<tr>
<th>This field</th>
<th>Displays the . . .</th>
</tr>
</thead>
<tbody>
<tr>
<td>Name</td>
<td>Name of the device file that is associated with the capacitor.</td>
</tr>
<tr>
<td>Mount type</td>
<td>Mounting style: <em>surface or leaded</em>.</td>
</tr>
<tr>
<td>Capacitance</td>
<td>Default nominal capacitance value as specified in the signal model.</td>
</tr>
<tr>
<td>Intrinsic inductance</td>
<td>Estimated Intrinsic inductance of a surface mounted capacitor computed from its height parameters. Intrinsic inductance computations do <em>not</em> account for the capacitor's mounting characteristics. You can experiment with different capacitor thickness settings. See <a href="#">Intrinsic Inductance</a> on page 28 for usage information.</td>
</tr>
<tr>
<td>Mounted inductance</td>
<td>Mounted inductance based on pin-escaping of a surface mounted capacitor and related via-to-plane characteristics. You can experiment with different mounted inductance parameters. See <a href="#">Mounted Inductance</a> on page 29 for usage information.</td>
</tr>
<tr>
<td>Resistance (ESR)</td>
<td>Signal model's impedance value at resonance.</td>
</tr>
<tr>
<td>Part Number</td>
<td>Part number that is saved to the capacitor's device file.</td>
</tr>
</tbody>
</table>
Intrinsic Inductance

SPECCTRAQuest Power Integrity can estimate the intrinsic inductance of a surface mounted capacitor based on the thickness (height) value that you supply.

➤ From the Decoupling Capacitor Editor, click Estimate adjacent to the Intrinsic inductance field (see Decoupling Capacitor Editor on page 26).

Table 2-1 Using the Decoupling Capacitor Editor

<table>
<thead>
<tr>
<th>This field . . .</th>
<th>Displays the . . .</th>
</tr>
</thead>
<tbody>
<tr>
<td>Package</td>
<td>Capacitor’s package symbol (.psm) as referenced by the capacitor’s device file.</td>
</tr>
</tbody>
</table>

Tip

If a library package is not suitable, click Create and specify the necessary parameters for creating a temporary package symbol.

See “Temporary Packages” on page 55 for more information.

Resonant frequency

Computed resonant frequency based on capacitance- and mounted and intrinsic inductance values.

Figure 2-11 Intrinsic Inductance Estimator
The intrinsic inductance estimation does not consider the capacitor’s mounting characteristics.

**Mounted Inductance**

SPECCTRAQuest Power Integrity can estimate the mounted inductance of a surface mounted capacitor based on the parameters that you supply. You specify a designated powerplane-pair, a package, and the side of the board on which to mount the capacitor.

---

**Tip**

Mounted inductance is the external loop inductance from the plane-pair including the 3-D path effects of etch length, via size, and loop area.

---

From the Decoupling Capacitor Editor, click *Estimate* adjacent to the Mounted inductance field (see *Decoupling Capacitor Editor* on page 26).

---

**Figure 2-12 Mounted Inductance Estimator:**
fixed plane-pair mode (left); experiment mode (right)

---

**Tip**

If a library package is not suitable, in the Package field click *Create* and specify the necessary parameters for a temporary package symbol. See “Temporary Packages” on page 55 for more information.
Additionally, you can use the *experiment* mode in which you can specify virtual planes with varied height and thickness parameters. You access *experiment* mode from the powerplane-pair drop-down list.

You use the mounted inductance estimator in conjunction with the *Use calculated cap-to-plane mounted inductances* fields of the Analysis Preferences dialog box. See Analysis Preferences on page 43 for more information.

➤ Click *Finish* to implement the database setup information and dismiss the setup wizard.
Power Integrity Design and Analysis

Topics in this chapter include

- **Powerplane Target Impedance** on page 32.
- **Single-Node Simulation** on page 33.
- **Analysis** on page 38.
- **Reports** on page 40.
- **Multi-Node Simulation** on page 42.
Powerplane Target Impedance

The key parameter in a power delivery system is the target impedance. Target impedance (\(Z_{\text{TARGET}}\)) is defined as:

\[
Z_{\text{target}} = \frac{(\text{Power Supply Voltage}) \times (\text{Ripple Tolerance})}{\text{Dynamic Current}}
\]

The power delivery system must deliver current at or near the target impedance at all frequencies from DC to the highest frequency of concern (often well into the microwave bands).

SPECCTRAQuest Power Integrity accurately models the VRM, capacitors, and system power and ground planes to determine the impedance of the power delivery system. Using SigWave, it presents a family of curves that describe impedance as a function of frequency at each cell on the PCB. These curves are plotted along with the power delivery system's target impedance. Those areas on the board where the power delivery system impedance exceeds the target impedance can be corrected by placing decoupling capacitors whose resonant frequencies effectively lower the system impedance to within the allowable target impedance.

SPECCTRAQuest Power Integrity computes the powerplane target impedance based on the bias voltage, tolerable ripple, and worst-case dynamic current. See “Running a single-node simulation” on page 34 for more information on establishing the target impedance for your system.
Single-Node Simulation

Overview

You run a single-node simulation to validate whether the number of capacitors that you chose can maintain the target impedance over the frequency band. Although decoupling capacitors are considered in single-node simulations, their placement is not. Multi-node simulation does consider decoupling capacitor placement as well as noise source placement (see Multi-Node Simulation on page 42).

In single-node simulation, SPECCTRAQuest Power Integrity wires all the decoupling capacitors in the worksheet (of the Power Integrity Design and Analysis dialog box, see Figure 3-2), whether they are placed or not, and the voltage regulator module (VRM) in parallel with a 1 amp AC current source. The equivalent circuit is represented in Figure 3-1.

![Figure 3-1 Single-Node Simulation Equivalent Circuit](image)

The results appear as an impedance versus frequency graph showing a composite impedance profile (see Figure 3-3 on page 38).
Running a single-node simulation

Once you have set up the board database, by running the setup wizard (see Using the Setup Wizard on page 14), you are ready to run a single-node simulation.

You set up and run simulations from the Power Integrity Design and Analysis dialog box (see Figure 3-2).

![Power Integrity Design & Analysis dialog box]

Figure 3-2  Power Integrity Design and Analysis dialog box

SPECCTRAQuest Power Integrity simulates on a plane-pair basis. Therefore, you start by selecting a plane-pair from the Power plane pair drop-down menu. Next, you specify a ripple tolerance and a maximum delta current. SPECCTRAQuest Power Integrity considers the parameters specified in the VRM as well. See Working with the Voltage Regulator Module on page 62 for more information.
SPECCTRAQuest Power Integrity then computes the powerplane target impedance based on variables that you specified (voltage, ripple tolerance, max delta current) and on the decoupling capacitors that you chose during library setup. These decoupling capacitors appear in the worksheet shown in Figure 3-2 on page 34.

For more information see

- **Powerplane Target Impedance** on page 32 for a discussion on target impedance.
- **Working in the worksheet** on page 36 for a discussion on worksheet cells.
- **Library Setup** on page 22 for a discussion on capacitor selection.

---

**Tip**

SPECCTRAQuest Power Integrity uses the capacitors that you selected during library setup to compute an initial estimate of the number of capacitors required. You can modify this estimate and run single-node simulations to evaluate the impedance profile as a function of frequency.

Finally, you click *Single Node Simulation*. The resulting waveforms soon display. You may also click *Report*. See **Analysis Waveforms** on page 38 and **Reports** on page 40.
Working in the worksheet

The Decoupling Capacitors field of the Power Integrity Design and Analysis dialog box (see Figure 3-2 on page 34) contains a worksheet. Table 3-1 describes how to interpret the cells in the worksheet. See Pre-Placement Operations on page 51 for information on placing decoupling capacitors.

Tip

While in the worksheet, SPECCTRAQuest Power Integrity makes extensive use of the context menu. When you select a row in the worksheet and right-click, the context pop-up menu lets you choose among different operations.

Table 3-1 Interpreting the worksheet (see Figure 3-2 on page 34)

<table>
<thead>
<tr>
<th>Column</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number Suggested</td>
<td>Based on the analysis conditions that you specified (capacitor selection, selected plane-pair, ripple tolerance, max delta current), SPECCTRAQuest Power Integrity suggests how many decoupling capacitors of each type are required to maintain the target powerplane impedance. If you change any of the analysis conditions, the target impedance will change; in turn, the Number Suggested will update accordingly.</td>
</tr>
<tr>
<td>Multiplier</td>
<td>A scaling factor for the Number Suggested. This product yields the Number to Analyze. In Figure 3-2 on page 34, notice that row 7 has a multiplier of 2 which effectively doubles the Number Suggested value to yield the Number to Analyze value. Conversely, row 9 has a multiplier of .5 which effectively halves the Number Suggested value to yield the Number to Analyze value. If you change any of the analysis conditions, the target impedance will change; in turn, the Number Suggested and the Number to Analyze will update accordingly.</td>
</tr>
<tr>
<td>Column</td>
<td>Function</td>
</tr>
<tr>
<td>--------------------</td>
<td>------------------------------------------------------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>Number to Analyze</td>
<td>The product of the Number Suggested and the Multiplier.</td>
</tr>
<tr>
<td>Device</td>
<td>The Allegro device name for each decoupling capacitor.</td>
</tr>
<tr>
<td>Value</td>
<td>The capacitance value of the decoupling capacitor as specified in the signal model.</td>
</tr>
<tr>
<td>Resonant Frequency</td>
<td>The computed resonant frequency (in Hertz), where $L$ is nominal inductance (in Henrys) and $C$ is capacitance (in Farads).</td>
</tr>
<tr>
<td></td>
<td>$f = \frac{1}{2\pi \sqrt{LC}}$</td>
</tr>
<tr>
<td>Number Unplaced</td>
<td>The number of decoupling capacitors that currently exist in the board database, but have not yet been placed in a physical location on the board.</td>
</tr>
<tr>
<td>Number to Create</td>
<td>The number of decoupling capacitors that do not exist in the board database; therefore, they must first be created (Number Suggested) and then they must be placed in a physical location on the board.</td>
</tr>
</tbody>
</table>

**Tip**

$\text{Number to Create} = (\text{Number Suggested}) - (\text{Number Unplaced}) - (\text{number existing and placed})$
Analysis

Both single- and multi-node simulations yield impedance versus frequency waveforms. You examine out-of-circuit analysis results (single-node simulation) to refine decoupling capacitor selection. You examine in-circuit analysis results (multi-node simulation) to refine decoupling capacitor placement.

Analysis Waveforms

![Single Node Simulation for Planes VCC2 – GND2](image)

**Figure 3-3  Analysis Waveforms: single-node simulation**

Figure 3-3 shows resulting waveforms from a single-node simulation. The blue colored waveform represents simulation of the VRM and the planes. Notice the high impedance at 14.80 MHz. The positive-going impedance to the left of 14.80 MHz is caused by the inductive nature of the VRM. The negative-going impedance to the right of 14.80 MHz is caused by the plane-pair going capacitive.

Also notice, however, that the waveform with decoupling capacitors exceeds the target impedance at 20.90 MHz. To correct this, you should add decoupling capacitors that resonate at this frequency.
Tip

Simulation reveals gaps in the frequency spectrum where the system impedance exceeds the target impedance. To address this, you should choose capacitors that resonate at frequencies in the area of concern and then re-simulate. See “Choosing a Decoupling Capacitor” on page 23 for information on capacitor selection.

Figure 3-4 Analysis Waveforms: multi-node simulation

Figure 3-4 shows the analysis results generated from a multi-node simulation. Notice that the waveforms exceed the target impedance in the frequency band immediately above and below 815.43 MHz. To correct this, you should add decoupling capacitors that resonate within this narrow frequency band.
Reports

SPECCTRAQuest Power Integrity captures many parameters about your design in a report. You can use this report at any point in the design cycle to assist you in your decisions about capacitor selection, plane-pair selection, simulation parameters, and placement strategies.

➤ To generate a report, click Report from the Power Integrity Design and Analyze dialog box. See Figure 3-5 on page 41 for an excerpt of a report.

The report includes . . .

■ Plane Layers
■ Board and plane layer size
■ Powerplane capacitance values
■ Resonant frequencies
  □ 1/2 wave
  □ 1/1 wave
  □ 3/2 wave
  □ 2/1 wave
  □ 5/2 wave
■ Ripple tolerance
■ Delta current
■ Target impedance
■ Detailed information on each decoupling capacitor, including
  □ number suggested
  □ multiplier
  □ number to analyze
  □ device
  □ capacitor value
  □ resonant frequency
- number to place
- number to create

- Detailed packaging information, including
  - device
  - package
  - part number
  - equivalent series resistance
  - intrinsic inductance
  - mounted inductance

- Noise sources (including distributed values and location on the board)
- VRM (including parameters and location on the board)
- Placed and unplaced capacitors (including their location on the board)

---

**Figure 3-5  Analysis Report** (partial)
Multi-Node Simulation

To obtain more accurate results, you can place decoupling capacitors, noise sources, and the VRM and then run a multi-node simulation over the full frequency domain. Unlike single-node simulation, where SPECCTRAQuest Power Integrity wires decoupling capacitors and the VRM in an ideal circuit with a constant current and voltage, multi-node simulation more accurately models the actual placement of these components in the physical design.

**Important**

SPECCTRAQuest Power Integrity exercises Multi-Node simulation with the Spectre circuit simulator. You must have Spectre installed and you must be licensed to use it.

Gridding Planes for Multi-node Simulation

SPECCTRAQuest Power Integrity divides plane-pairs into a user-defined grid size. See the Working with Analysis Preferences table on page 44 for information on setting the multi-node grid size. SPECCTRAQuest Power Integrity characterizes each mesh point as four connected transmission lines which are derived from the board outline and the layer stack up.

![Multi-node grid size with 8x8 meshing](image)

**Figure 3-6** Multi-node grid size with 8x8 meshing

Any decoupling capacitors, voltage regulator modules, or noise sources that you place align with a mesh point. Upon multi-node simulation, SPECCTRAQuest Power Integrity generates a waveform for each node point.
Analysis Preferences

Before running multi-node simulations, you should review or modify the default settings in the Analysis Preferences dialog box.

- From the Power Integrity Design and Analysis dialog box (see Figure 3-2 on page 34), click Preferences.

The Analysis Preferences dialog box appears. The Working with Analysis Preferences table on page 44 describes each field in this dialog box.

![Analysis Preferences dialog box]

Figure 3-7 Analysis Preferences dialog box
<table>
<thead>
<tr>
<th>In this field</th>
<th>You specify . . .</th>
</tr>
</thead>
<tbody>
<tr>
<td>Multi-node grid size</td>
<td>The granularity with which SPECCTRAQuest Power Integrity meshes planes during multi-node analysis. See Gridding Planes for Multi-node Simulation on page 42.</td>
</tr>
<tr>
<td>Min plane/board area</td>
<td>The minimum area of a shape on a conductor layer. See DC Net/Plane Association on page 19.</td>
</tr>
<tr>
<td></td>
<td>During analysis, SPECCTRAQuest Power Integrity always considers shapes on plane layers.</td>
</tr>
<tr>
<td></td>
<td>This field works in conjunction with the include planes on conductor layers field, below.</td>
</tr>
<tr>
<td>Include planes on conductor</td>
<td>Whether to include conductor layers in analysis. When 'checked' SPECCTRAQuest Power Integrity considers conductor layers in analysis.</td>
</tr>
<tr>
<td>layers</td>
<td>This field works in conjunction with the Min plane/board field, above.</td>
</tr>
</tbody>
</table>
Table 3-2 Working with Analysis Preferences

<table>
<thead>
<tr>
<th>In this field . . .</th>
<th>You specify . . .</th>
</tr>
</thead>
<tbody>
<tr>
<td>Use calculated cap-to-plane mounted inductance</td>
<td>Whether to use calculated mounted inductance values specified in the Decoupling Capacitor Editor. See Modifying a Decoupling Capacitor on page 26. When you initiate a mounted inductance estimate, from the Decoupling Capacitor editor, SPECCTRAQuest Power Integrity evaluates the physical mounting parasitics of each capacitor type, such as the height of the capacitor and the distance between planes. These estimates are then saved in resident-memory. With Use calculated cap-to-plane mounted inductance enabled, SPECCTRAQuest Power Integrity reads the stored mounted inductance estimates from resident-memory instead of having to re-calculate them on subsequent simulations. If you modify the active plane-pair, or if you choose a different plane-pair, these values are lost from resident-memory. You will have to re-calculate the mounted inductance for each type of capacitor. When the number of pending calculations exceeds three, a confirmer prompts you as follows: ➤ Choose yes to proceed with a new calculation -or- ➤ Choose no to continue with the values stored in memory.</td>
</tr>
<tr>
<td>Upper analysis limit</td>
<td>The upper frequency range of the simulation.</td>
</tr>
<tr>
<td>Lower analysis limit</td>
<td>The lower frequency range of the simulation.</td>
</tr>
<tr>
<td>Simulator</td>
<td>The simulator. Spectre is the only choice. More simulators may be available in future releases.</td>
</tr>
</tbody>
</table>
**Table 3-2 Working with Analysis Preferences**

<table>
<thead>
<tr>
<th>In this field . . .</th>
<th>You specify . . .</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage</td>
<td>This field is for future use.</td>
</tr>
<tr>
<td>Temperature</td>
<td>This field is for future use.</td>
</tr>
</tbody>
</table>

**Placing Components**

In multi-node simulation, you place the voltage regulator module, noise sources, and decoupling capacitors.

Tip

Component placement makes extensive use of the context pop-up menu. Depending on what is selected, in either the Power Integrity Design and Analysis dialog box or in the board layout, yields a context pop-up menu with access to common commands.

The sections that follow explain the placement process.
Placing the Voltage Regulator Module (VRM)

Before you run multi-node simulations, you must place a voltage regulator module (VRM) in the board layout. You can vary the parameters of the VRM for each selected plane-pair.

➤ In the board layout, right-click and choose **VRM Location** from the context pop-up menu.

VRMs appear in the board layout as a graphic on the analysis layer and disappear when you dismiss the Power Integrity Design and Analysis dialog box.

![VRM placed in the board layout](image)

**Figure 3-8  VRM placed in the board layout**

Once placed, you can edit, move, or delete a VRM.

➤ In the board layout, click on a VRM and choose **Delete, Edit, or Move** from the context pop-up menu.

See **Voltage Regulator Module (VRM)** on page 61 for information on editing the VRM.
Placing Noise Sources

Before you run multi-node simulations, you must place noise sources in the board layout.

➤ Enter a delta current value, click OK, then right-click in the board layout and choose Add Noise Source from the context pop-up menu.

The noise source symbol attaches to your cursor for placement. See Figure 3-8 on page 48.

![Add Noise Source dialog box](image)

**Figure 3-9 Add Noise Source dialog box**

When adding a noise source, or moving one a new location, the context pop-up menu lets you choose to attach the noise source to a nearby component or to place it wherever you want.

You can add as many noise sources as required within your established noise budget. You should allot suspect areas on the board higher noise contributions.

⚠️ **Important**

You cannot create a zero-Ampere noise source.

Noise sources appear in the board layout on the analysis layer and disappear when you dismiss the Power Integrity Design and Analysis dialog box.
Noise sources placed in the board layout

Once placed, you can edit, move, or delete a noise source.

➤ In the board layout, click on a noise source and choose Delete, Edit, or Move from the context pop-up menu.

When a noise source is associated with a component and that component is moved or deleted, the noise source follows.
Placing Decoupling Capacitors

Before placing decoupling capacitors in the board layout, you should run multi-node simulations to discern the frequencies that need attention. The Context menu operations for decoupling capacitors (pre-placement) table on page 52 and the Context menu operations for decoupling capacitors (post-placement) table on page 53 describe placement operations.

**Important**

When placing decoupling capacitors, SPECCTRAQuest Power Integrity ignores spacing and position conflicts. They will, however, be flagged as DRCs update.
As you place a decoupling capacitor, an enveloping circle represents its effective radius. This radius is based on a fraction of the resonant frequency's wavelength for the decoupling capacitor, which you set in the control panel (see Figure 3-11 on page 50). This lets you quickly determine how close to place high frequency capacitors to noise sources.

**Tip**

With such a large radius, low frequency decoupling capacitors can be effective when placed anywhere on the board.

The capacitor's effective radius circle appears on the analysis layer. When the capacitor is deselected, the circle disappears. The graphics only appear while the Power Integrity Design and Analysis dialog box is active.

When SPECCTRAQuest Power Integrity creates a decoupling capacitor, it connects it to the proper signal nets and it routes it based on its package definition. Packages for most decoupling capacitors have connections in the package; therefore, they are routed when placed.

After SPECCTRAQuest Power Integrity places a component, a new component of the same type attaches to the cursor until the number of unplaced capacitors is zero. You can right-click and choose *Stop Placement* context pop-up menu item to halt placement.

**Pre-Placement Operations**

You can perform the following operations on a decoupling capacitor.

- In the worksheet (see Figure 3-2 on page 34), click in any cell in a row, then right-click and choose *Place* from the context pop-up menu. As the decoupling capacitor's symbol attaches to your cursor, the following operations (a second right-click) are available to you.
Table 3-3  Context menu operations for decoupling capacitors (pre-placement)

<table>
<thead>
<tr>
<th>This Operation</th>
<th>Will . . .</th>
</tr>
</thead>
<tbody>
<tr>
<td>Place</td>
<td>Attach the next available decoupling capacitor to the cursor for placement in the board layout.</td>
</tr>
<tr>
<td></td>
<td>SPECCTRAQuest Power Integrity places unplaced devices—devices which exist in the design but do not have locations in the board layout—first.</td>
</tr>
<tr>
<td></td>
<td><strong>Important</strong></td>
</tr>
<tr>
<td></td>
<td>A decoupling capacitor must have an associated package before it is placed in the physical board layout.</td>
</tr>
<tr>
<td></td>
<td>You are warned when attempting to place an unpackaged decoupling capacitor.</td>
</tr>
<tr>
<td></td>
<td>- See <a href="#">Modifying a Decoupling Capacitor</a> on page 26 for information on changing the assigned package.</td>
</tr>
<tr>
<td></td>
<td>- See <a href="#">Temporary Packages</a> on page 55 for more information on creating a temporary package.</td>
</tr>
<tr>
<td>Stop Placement</td>
<td>Stop placement and remove the unplaced package symbol from the cursor. The worksheet in the Power Integrity Design and Analysis dialog box moves forward.</td>
</tr>
<tr>
<td>Next Capacitor Type</td>
<td>Select the next capacitor type in the worksheet in the Power Integrity Design and Analysis dialog box. Therefore, the current unplaced package symbol replaces the next capacitor type (from the next row in the worksheet) on your cursor.</td>
</tr>
</tbody>
</table>
Post-Placement Operations

Once placed, you can perform the following operations on a decoupling capacitor.

➤ In the board layout, click on a decoupling capacitor, then right-click and choose from the following operations listed in the context pop-up menu

Table 3-4  Context menu operations for decoupling capacitors (post-placement)

<table>
<thead>
<tr>
<th>This Operation</th>
<th>Will . . .</th>
</tr>
</thead>
<tbody>
<tr>
<td>Unplace</td>
<td>Remove the decoupling capacitor from the surface of the board layout but not delete it from the design. Therefore, it becomes an unplaced component. This is also reflected in the Number Unplaced column in the appropriate row in the worksheet.</td>
</tr>
<tr>
<td>Move</td>
<td>Place the component on the cursor. When you click elsewhere in the board layout, the component relocates.</td>
</tr>
<tr>
<td>Rotate</td>
<td>Rotate the selected component 180 degrees.</td>
</tr>
<tr>
<td>Delete</td>
<td>Remove the decoupling capacitor from the design. This is also reflected in the Number to Create column in the appropriate row in the worksheet.</td>
</tr>
<tr>
<td>Edit</td>
<td>Invoke the Decoupling Capacitor Editor. See Modifying a Decoupling Capacitor on page 26 for more information.</td>
</tr>
<tr>
<td>Mounted Inductance</td>
<td>Perform an in-circuit estimate of the mounted inductance parasitics of the selected decoupling capacitor. See Mounted Inductance on page 29 for more information.</td>
</tr>
<tr>
<td>Cross Probe</td>
<td>Let you view the simulation waveform associated with the selected mesh area containing the decoupling capacitor. See Crossprobing on page 54 for more information.</td>
</tr>
</tbody>
</table>
Crossprobing

You can crossprobe between analysis results in the waveform window and the corresponding mesh area in the board layout. Conversely, you can click on a mesh area in the board layout and the corresponding waveform highlights in the waveform viewer—SigWave.

Tip

Each waveform is the result of simulation within a node mesh point on the board. See Gridding Planes for Multi-node Simulation on page 42 for more information on node mesh points.

➤ Click on a multi-node simulation waveform and the corresponding mesh area highlights in the board layout.

➤ Click on a capacitor in a mesh area in the board layout, then right-click and choose crossprobe from the context pop-up menu. The corresponding waveform highlights in SigWave.

Figure 3-12 Crossprobing a simulation waveform to placement in board layout
Temporary Packages

Topics in this appendix include

- Overview on page 56.
- Creating Temporary Surface Mounted Packages on page 56.
- Creating Temporary Leaded Packages on page 59.
Overview

A decoupling capacitor must have an associated package before it is placed on the board. SPECCTRAQuest Power Integrity's flexibility lets you experiment with various capacitor packages. The fields available in the temporary package editor depend on the pin type of the capacitor: *surface mounted* or *leaded*.

The temporary package editor appears automatically if you attempt to place an unpackaged decoupling capacitor. Additionally, you can access the temporary package editor as follows:

- From the Power Integrity Design and Analysis dialog box, click on a capacitor in the worksheet, then choose *Edit* from the context pop-up menu. Next, click the Package field in the Decoupling Capacitor Editor.

- From the Library Setup screen of the setup wizard, click on a decoupling capacitor in the library tree, right-click and choose *Edit* from the context pop-up menu, then click the Package field in the Decoupling Capacitor Editor.

Creating Temporary Surface Mounted Packages

When you choose *Surface* in the Mount Type field of the Decoupling Capacitor Editor, the temporary package editor that appears is described in Figure A-1 on page 57 and in Table A-1 on page 57.
**Figure A-1** Surface Mounted Temporary Packages

**Table A-1** Temporary Packages: surface mounted

<table>
<thead>
<tr>
<th>In this field . . .</th>
<th>You specify . . .</th>
</tr>
</thead>
<tbody>
<tr>
<td>Name</td>
<td>The name of the package. Initially, this field displays the name of the selected capacitor in the Decoupling Capacitor Editor or the name of the selected capacitor in the Power Integrity Design and Analysis dialog box.</td>
</tr>
<tr>
<td>Type</td>
<td>A capacitor type as specified in the <code>cap_sizes.dat</code> file.</td>
</tr>
<tr>
<td>Length</td>
<td>A physical dimension. You can edit this field only when <code>other</code> appears in the <code>type</code> field. Otherwise, the actual dimension of the selected capacitor appears.</td>
</tr>
<tr>
<td>Width</td>
<td>A physical dimension. You can edit this field only when <code>other</code> appears in the <code>type</code> field. Otherwise, the actual dimension of the selected capacitor appears.</td>
</tr>
<tr>
<td>Pin Width</td>
<td>A physical dimension.</td>
</tr>
<tr>
<td>Via Diameter</td>
<td>A physical dimension.</td>
</tr>
<tr>
<td>Etch Width</td>
<td>A physical dimension.</td>
</tr>
</tbody>
</table>
When SPECCTRAQuest Power Integrity creates a via, it creates a corresponding padstack as well. If the via is within the pad, the top and the bottom padstack layers are the same size as the via. If the via is outside of the pad, as with a cline connection, the top and the bottom padstack layers are 10 Mils larger in diameter.

- **Pkg Side**
  
  Both, Left, or Right

- **X Offset to Via**
  
  The horizontal distance from the pin breakout to the via. A positive value is the direction out from the body of the capacitor: left on the left side, right on the right side. A negative value is in the opposite direction, into or through the body of the capacitor.

- **Y Offset to Via**
  
  The vertical distance from the pin breakout to the via. A positive value is up from the pin center; a negative value is down.

- **Y Offset to Breakout**
  
  The vertical distance from the center of the pin to the etch breakout from the pin. A positive value is up from the center of the pin; a negative value is down. You must limit the breakout value to the size of the pin.

- **Add Pin Escape**
  
  Additional pin escapes. By default, SPECCTRAQuest Power Integrity adds pin escapes after the selected row. If a pin escape is not selected, SPECCTRAQuest Power Integrity adds the new pin escape to the bottom of the list. New pin escapes have the following default values:

  - **Pkg Side** = Both
  - **X offset** = 50 Mils
  - **Y offset** = 0 Mils
  - **Y offset to breakout** = 0 Mils

- **Delete Pin Escape**
  
  Delete the selected pin escape
Creating Temporary Leaded Packages

When you choose *Leaded* in the Mount Type field of the Decoupling Capacitor Editor, the temporary package editor that appears is described in Figure A-2 on page 59 and in Table A-2 on page 59.

![Create Leaded Mount Capacitor Temporary Package](image)

**Figure A-2**  Leaded Temporary Packages

**Table A-2**  Temporary Packages: leaded

<table>
<thead>
<tr>
<th>In this field...</th>
<th>You specify...</th>
</tr>
</thead>
<tbody>
<tr>
<td>Name</td>
<td>The name of the package. Initially, this field displays the name of the selected capacitor in the Decoupling Capacitor Editor or the name of the selected capacitor in the Power Integrity Design and Analysis dialog box.</td>
</tr>
<tr>
<td>Length</td>
<td>A physical dimension</td>
</tr>
<tr>
<td>Width</td>
<td>A physical dimension</td>
</tr>
<tr>
<td>Pin Width</td>
<td>A physical dimension</td>
</tr>
</tbody>
</table>
Voltage Regulator Module (VRM)

Topics in this appendix include

- Working with the Voltage Regulator Module on page 62.
- Voltage Regulator Module Editor on page 63.
Working with the Voltage Regulator Module

Before SPECCTRAQuest Power Integrity performs single- or multi-node analysis, you must define parameters for, and later place, a voltage regulator module (VRM). See Placing the Voltage Regulator Module (VRM) on page 47 for instructions on placing a VRM in your design.

Tip
VRMs act as supply points from which power is delivered to the plane and regulated.

A voltage regulator module converts one DC voltage to another DC voltage. The VRM uses a reference voltage and feedback loop to sense the voltage near the load and it adjusts the current, accordingly.

SPECCTRAQuest Power Integrity models the behavior of the VRM as a four-element SPICE model.
Voltage Regulator Module Editor

➤ You access the voltage regulator module editor from the Power Integrity Design and Analysis dialog box (choose Analyze – Power Integrity).

Tip

SPECCTRAQuest Power Integrity analyzes on a plane-pair basis. Therefore, you may want to change the parameters of the VRM as you choose among different plane-pairs.

The Voltage Regulator Module Editor figure on page 64 and the VRM Editor (including input inductance fields) table on page 64 describe the fields in the voltage regulator module editor.
Figure B-1 Voltage Regulator Module Editor

Table B-1 VRM Editor (including input inductance fields)

<table>
<thead>
<tr>
<th>In this field . . .</th>
<th>You specify the . . .</th>
</tr>
</thead>
</table>

Voltage Regulator Module Editor Fields

Slew Inductance: Rate at which the VRM can react to changes in current. Example: a VRM may take 15 microseconds to slew the current from 8- to 20-amps.

Flat Resistance: Equivalent series resistance of the capacitor that is associated with the VRM.
Table B-1  VRM Editor (including input inductance fields)

<table>
<thead>
<tr>
<th>In this field</th>
<th>You specify the . . .</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Inductance</td>
<td>Cable or pin parasitic inductance of connecting the VRM to the board.</td>
</tr>
<tr>
<td>Output Resistance</td>
<td>Sense resistance between the VRM and the load.</td>
</tr>
<tr>
<td>Voltage</td>
<td>The potential difference between the plane pairs.</td>
</tr>
<tr>
<td>Ripple Tolerance</td>
<td>The maximum voltage droop or spike noise that the design can tolerate (expressed as a percentage of voltage).</td>
</tr>
<tr>
<td>Ramp Time</td>
<td>The maximum time for the VRM to react to a transient current.</td>
</tr>
<tr>
<td>Ramp Current</td>
<td>The maximum transient current. This value is usually the same as the delta current value that you specify in the Power Integrity Design and Analysis dialog box.</td>
</tr>
</tbody>
</table>